SE Laboratories
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MODEL 350D

MODEL 351D

Autohet Frequency Counters

Operating & Service Manual

MODEL 350D
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Autohet Frequency Counters
Operating & Service Manual

Serial Prefix/CCN Group beginning:
120, 220, 318, 910, 010

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CERTIFICATION

EIP Incorporated certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

WARRANTY

EIP Incorporated warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Incorporated will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or its authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied. EIP Incorporated and Danalab Incorporated, are not liable for consequential damages.

ASSISTANCE

For assistance, contact the EIP representative in your area, or EIP Incorporated.

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SECTION 1

GENERAL INFORMATION & SPECIFICATIONS

1-1. DESCRIPTION

1-2. The EIP 350D/351D series of Autohet Frequency Counters automatically measure the frequency of any CW signal within the range of 20 Hz to 12.4 GHz (350D), or 20 Hz to 18.0 GHz (351D). In both series, this frequency is covered in three bands: 20 Hz to 300 MHz, 100 MHz to 850 MHz, and 825 MHz to 12.4 GHz, or 18.0 GHz.

1-3. Measurements in Band I (20 Hz to 300 MHz) are made with a 300 MHz direct electronic counter. Band II (100 MHz to 850 MHz) uses a prescaler to divide the input signal by a factor of four into the frequency range of the 300 MHz direct counter. Band III (825 MHz to 12.4/18.0 GHz) measurements are made by heterodyning the input frequency with an automatically selected harmonic of an internal 200 MHz comb generator, producing a difference frequency which falls within the range of the 300 MHz direct counter. The inacuracy of the indicated reading by the counter, is directly related to the quality of the Time Base Oscillator over the entire operating range of the counter (see Sections 1 and 6).

1-4. The display on the 350D/351D Counters gives a direct readout of the measured frequency over the entire operating range of the counter. The counter also includes automatic suppression of leading zeros, except during a no signal input condition.

1-5. The frequency readout of the 350D/351D Counters is displayed in a fixed position format that is conveniently sectionalized in GHz, MHz, kHz, and Hz. Four gate times: 1 ms, 10 ms, 100 ms, and 1 sec., are automatically selected depending upon the setting of the RESOLUTION switch.

1-6. For applications where less resolution is required, pushbutton display blanking (RESOLUTION) is provided to simplify the readout.

1-7. To assure trouble-free performance, the 350D/351D Counters are completely solid-state. For ease of repair and maintenance, the major portion of the counter circuitry is contained on plug-in printed circuit boards or in easily removed modules. Special test points allow monitoring of critical circuit functions.

1-8. INSTRUMENT IDENTIFICATION

1-9. All models of the 350D/351D series Counters are identified by two number sets: the Model and Configuration Control Number (e.g: 351D-CCN101), and a specific Serial Number (e.g: 12345 or 101-12345). Both sets of numbers should be mentioned in any correspondence regarding the counter.

1-10. SPECIFICATIONS

1-11. EIP 350D/351D Autohet Frequency Counter specifications are given in Table 1-1.

NOTICE

"AUTOHET" is a registered trademark of EIP Inc.

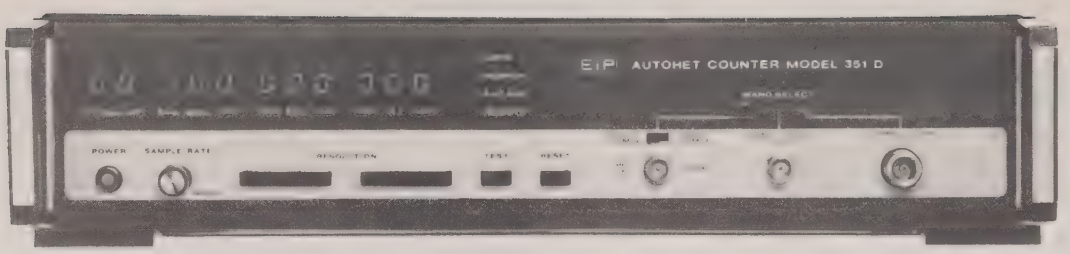


FIGURE 1-1. FRONT VIEW - 351D AUTOHET FREQUENCY COUNTER

TABLE 1-1. SPECIFICATIONS - 350D/351D COUNTERS

GENERAL:

Frequency Range:	20 Hz - 12.4 GHz (Model 350D); 20 Hz - 18.0 GHz (Model 351D).
Accuracy:	±1 count ± time base accuracy.
Resolution:	1 Hz to 1 MHz in decade steps.
Gate Time:	1 sec (1 Hz), 0.1 sec (10 Hz), 10 ms (100 Hz), 1 ms (1 kHz, 10 kHz, 100 kHz, 1 MHz). Band II gate times are expanded by four.
Sample Rate:	Variable, 100 ms to 10 seconds.
Display:	11 digit light-emitting diode (LED); sectionalized to read: GHz, MHz, kHz, and Hz.
Operation:	Completely automatic after setting input selector.
Acquisition Time:	In Band III, comb line acquisition requires 10 ms/GHz plus 40 ms (nominal). Once locked to a comb line, readings can be taken at rate of selected gate time.
Operating Temp:	0° to +50°C.
Power:	115 Vac or 230 Vac, ±10%, 50-60 Hz, 80 watts.
Weight:	Shipping: 30.0 lbs (13.6 kg); Net: 25.5 lbs (11.6 kg).
Access. Furnished:	Detachable power cord, 8 ft (241 cm) long, with plug. Operating & Service manual.
Access. Available:	Rack Mount Kit: P/N: 101054. Carrying Case: P/N: 5700001.

CONTROLS:

See Figures 3-1 and 3-2, and Tables 3-1 and 3-2.

TIME BASE (STANDARD):

Crystal Frequency:	10 MHz.
Stability:	
Aging Rate:	$< \lvert 3 \times 10^{-7} \rvert$/month.
Short Term:	$< 1 \times 10^{-9}$ rms for one second averaging time.
Temperature:	$< \lvert 2 \times 10^{-6} \rvert$ between 0° to +50°C.
Line Variation:	±10% line voltage change results in a frequency shift of $< \lvert 1 \times 10^{-7} \rvert$.
Warm-up Time:	None.
Output Freq:	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
Ext. Time Base:	Requires 10 MHz, 1 V p-p minimum into 300 ohms.

SIGNAL INPUTS:

BAND IA:

Frequency Range:	20 Hz - 135 MHz
Min. Sensitivity:	25 mV rms
Input Impedance:	1 megohm/20 pf
Maximum Input:	3 V rms
Max. Input without Damage:	150 V rms (Note 1)
Coupling:	AC
Connector:	BNC female

Note 1: Above 1 kHz maximum input decreases at 6 dB/octave rate to 3.0 V rms at 40 kHz.

BAND IB:

Frequency Range:	10 MHz - 300 MHz
Min. Sensitivity:	-20 dBm (22 mV rms)
Input Impedance:	50 ohms nominal
Maximum Input:	+10 dBm (0.7 V rms)
Max. Input without Damage:	+27 dBm (5.0 V rms)
Coupling:	AC
Connector:	BNC female

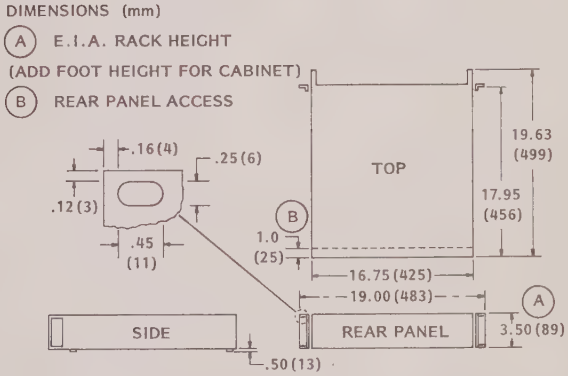
BAND II:

Frequency Range:	100 MHz - 850 MHz
Min. Sensitivity:	100 MHz - 150 MHz: -15 dBm (40 mV rms) 150 MHz - 850 MHz: -20 dBm (22 mV rms)
Maximum Input:	+10 dBm (0.7 V rms)
Max. Input without Damage:	+27 dBm (5.0 V rms)
Input Impedance:	50 ohms nominal
Coupling:	AC
Connector:	BNC female

BAND III:

Frequency Range:	825 MHz - 12.4 GHz (350D) 825 MHz - 18.0 GHz (351D)
Min. Sensitivity:	825 MHz - 1.1 GHz: -20 dBm (22 mV rms) 1.1 GHz - 12.4 GHz: -25 dBm (12 mV rms) 12.4 GHz - 18.0 GHz: -20 dBm (22 mV rms)
Maximum Input:	+7 dBm (0.5 V rms)
Max. Input without Damage:	+20 dBm (2.2 V rms)
Input Impedance :	50 ohms nominal
Coupling:	DC to source, AC to counter
Connector:	N Precision female
VSWR:	2.5 : 1 (typical)
FM Tolerance:	40 MHz p-p, worst case, for modulation rates from DC to 10 MHz.

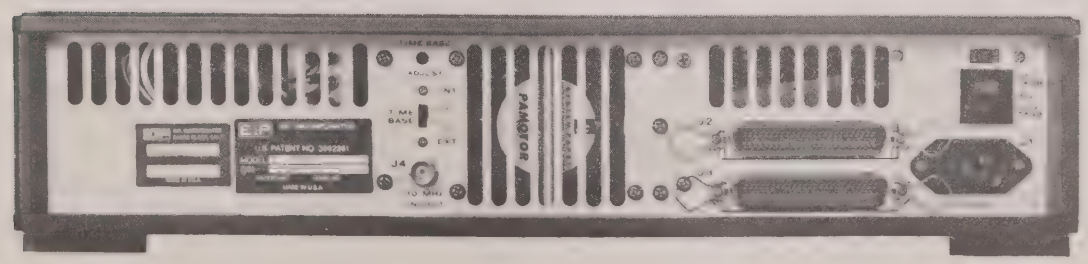
DIMENSIONS (mm)



All specifications subject to change at manufacturers discretion.

TABLE 1-1 (Continued). SPECIFICATIONS - 350D/351D COUNTERS

FIGURE 1-2. REAR VIEW - 351D AUTOHET FREQUENCY COUNTER



SECTION 2

INSTALLATION

2-1. UNPACKING

2-2. The EIP 350D/351D series of Autohet Frequency Counters arrive ready for operation. Carefully inspect the shipping carton before opening for any evidence of visible or concealed damage. If any seems apparent, ask that the shipper's agent be present when the instrument is unpacked.

2-3. Remove the packing carton and supports, being careful not to scar or damage the instrument. Make a complete visual inspection of the counter, checking for any damage or missing components. Check that all switches and controls operate mechanically. Report any damage to EIP immediately.

2-4. INSTALLATION

2-5. There are no special installation instructions for the 350D/351D Counters. The units are self-contained bench or rack mounted instruments, which only require connection to a standard, single-phase, 115/230 V, 50-60 Hz power line for operation. CAUTION: Check current rating of counter fuse and setting of rear panel 115/230 Vac slide switch before applying power to counter.

2-6. INCOMING OPERATIONAL CHECK

2-7. The following procedure outlines an operational check of the counter which may be conducted without special tools, signal generators, or test equipment. The internal TIME BASE CLOCK is used as the input signal to the 300 MHz counter, therefore it cannot check the operation of the Band II prescaler or the Band III comb generator.

a. Turn counter POWER switch off. Check fuse rating and setting of 115/230 switch (on rear panel).

b. Connect counter power cord to a source of 115 or 230 V, 50-60 Hz, single-phase power. The ground terminal on the power cord plug should connect to a reliable earth ground.

c. Press POWER switch (on front panel) to turn counter on. The counter display should light, and the internal cooling fan should operate.

d. Place the rear panel TIME BASE INT/EXT switch in the INT position.

e. Partially depress any one of the RESOLUTION switches and release it so no switch remains in the depressed position. All digits in the 11-digit display should indicate "0" (zero).

f. Depress the TEST switch on the front panel. The display should indicate 10 000 000 (10 MHz). Note that the three leading zeros are blanked (not lit).

g. Blank the 1 Hz digit by pressing the right hand RESOLUTION switch.

h. Depress the TEST button again. The display should still indicate 10 MHz, but with the final "0" blanked. Also note a decrease in the gate time evidenced by the shorter on-time of the GATE light.

i. Test each RESOLUTION switch in turn, starting with the 1 Hz digit. Note that the digit immediately above that switch, and all digits to the right of that switch, are blanked.

j. Unblank all display digits (see "e." above for procedure).

k. With no input signal, the entire display should show all zeros in all positions of the BAND SELECT switch.

l. Depress both the TEST and RESET switches simultaneously. All display digits should show "8" (all segments of each display lighted).

m. This completes the counter confidence check. All CW signals within the frequency range of the counter may be counted as required. Refer to Section 1 for proper signal levels. If the counter fails to perform as described above, refer to Section 5.

SECTION 3

OPERATION

3-1. INTRODUCTION

3-2. The operation of the counter is completely automatic after selecting the appropriate operating band. Controls and indicators have been kept to a minimum to insure simple, error-free performance.

3-3. CONTROLS, INDICATORS AND CONNECTORS

3-4. Front panel controls, indicators and connectors are shown in Figure 3-1 and described in Table 3-1. Rear panel controls and connectors are shown in Figure 3-2 and described in Table 3-2.

3-5. VISUAL DISPLAY (LED) BRIGHTNESS ADJUSTMENT

3-6. Apparent brightness of the light-emitting diode (LED) numerical display may be varied by adjustment of potentiometer A103R22. (R22 is located near the top front of PC Board A103, and is accessible by removing the top cover of the counter.) Adjust R22 clockwise to increase display brightness, or counter-clockwise to decrease the brightness.

WARNING

DO NOT APPLY A SIGNAL EXCEEDING THE MAXIMUM INPUT SPECIFICATION TO ANY INPUT. EXTENSIVE DAMAGE NOT COVERED BY THE WARRANTY WILL OCCUR, WHETHER OR NOT THE COUNTER IS TURNED ON, TURNED OFF OR APPEARS TO BE INOPERATIVE!

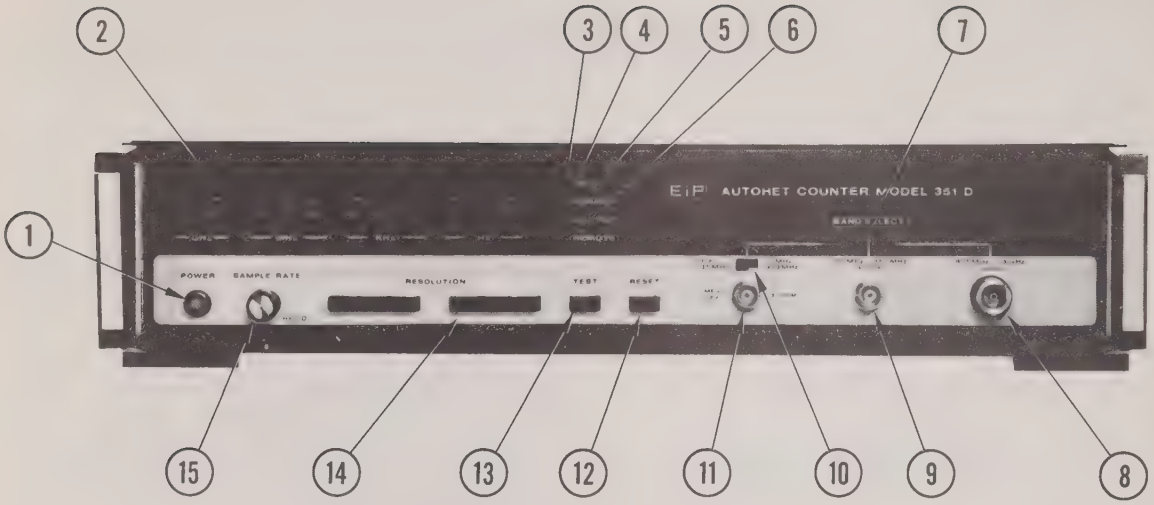


FIGURE 3-1. FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

TABLE 3-1. FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

ITEM NO.	ITEM	FUNCTION
(1)	POWER On/Off Switch	Turns counter power on and off.
(2)	Visual Display	The 11-digit LED (light-emitting diode) display provides a direct numerical readout of the input frequency. The display is conveniently sectionalized into GHz, MHz, kHz, and Hz.
(3)	GATE Indicator	Lights when signal gate is open.
(4)	SEARCH Indicator	Provides visual indication that the Band III Converter is not locked onto an input signal.
(5)	EXT REF Indicator	Lights when counter is set to EXT REF (external reference) mode via rear panel switch. CAUTION: Lamp does not indicate level of external reference signal.
(6)	REMOTE Indicator	Used only with Option 07 - Remote Programming (refer to Section O - Options).

TABLE 3-1 (Continued). FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

ITEM NO.	ITEM	FUNCTION
7	BAND SELECT Switch	This switch determines the operating frequency range of the counter. Band I: Placing the BAND SELECT switch in the fully left position, allows two modes of measurement: 20 Hz - 135 MHz with 1 megohm/20 picofarad input impedance, and 10 MHz - 300 MHz with a 50 ohm input impedance. The position of the Band I Mode switch (Item 10) determines which mode is selected. Band II: Placing the BAND SELECT switch in the center position allows frequency measurements in the 100 MHz - 850 MHz range with 50 ohm input impedance. Band III: Placing the BAND SELECT switch in the fully right position allows frequency measurements in the 825 MHz - 12.4 GHz range (350D), or 825 MHz - 18.0 GHz range (351D) with 50 ohm impedance.
8	Band III Input Connector	Precision type N female. CAUTION: see WARNING notice in Section 3 regarding maximum input levels.
9	Band II Input Connector	Type BNC female.
10	Band I Mode Switch	The position of this switch determines which mode of Band I is selected: either the high impedance (20 Hz - 135 MHz) mode, or the 50 ohm (10 MHz - 300 MHz) mode.
11	Band I Input Connector	Type BNC female.
12	RESET Switch ▲	The manually operated RESET pushbutton overrides all controls, resets the counter and Autohet Converter, and initiates a new reading.
13	TEST Switch ▲	Depressing the TEST pushbutton places the counter in a self-test mode. It applies a signal derived from the 10 MHz Time Base Oscillator to the counter. The proper display in the TEST mode is 10 000 000 (10 MHz).
14	RESOLUTION Switches	Six pushbutton switches allow blanking (turning off) of the six least significant digits in the visual display. Each switch blanks the digit above, and all digits to the right of that switch. Four gate times appropriate to the required resolution are also selected. 1 Hz resolution is achieved by partially depressing and releasing one of the switches (this action releases all the switches).
15	SAMPLE RATE/ HOLD Control	Continuously variable control for one-tenth to ten seconds per reading, with 1 ms. gate time. (Gate time is added to sample time, thus minimum reading time in 1 second gate position is 1.1 second.) Last reading retained indefinitely in HOLD.

▲ VISUAL DISPLAY TEST: Depressing both the TEST and RESET pushbuttons simultaneously, will cause all display digits to show the numeral "8" (all segments of each digit lighted).

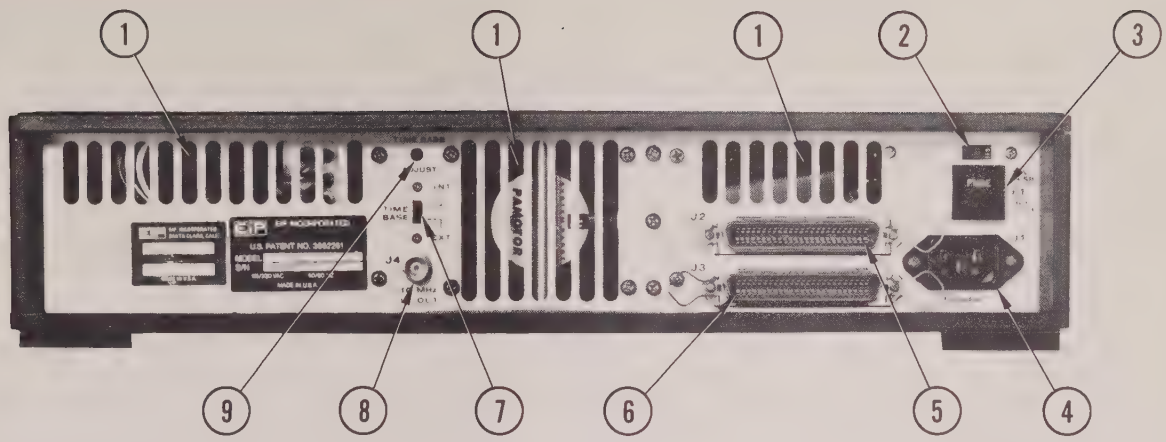


FIGURE 3-2. REAR PANEL CONTROLS AND CONNECTORS

TABLE 3-2. REAR PANEL CONTROLS AND CONNECTORS

ITEM NO.	ITEM	FUNCTION
1	Air passage openings for cooling fan	An internal fan moves cooling air through the counter. Do not allow anything to block openings which might restrict air flow.
2	115/230 Switch	Sets operating voltage of counter to match power line. CAUTION: Be sure 115/230 switch setting and fuse rating match power line voltage.
3	Fuse Holder	Fuse provides overload protection for the counter. Use only a 1.5 A, Slow-Blow, 3AB/MDX type fuse for 115 Vac operation, or a 0.75 A, Slow-Blow, 3AB/MDL type fuse for 230 Vac operation.
4	AC POWER Connector Connector	Accepts AC power cord supplied with counter.
5	BCD OUTPUT Connector (Option 09)	Used with Option 09 - BCD Output. Refer to Section O - Options, for complete description.
6	REMOTE PROGRAMMING Connector (Options 01, 06, 07)	Used with Option 01 - Programmable YIG Preset, Option 06 - Programmable Offsets, and Option 07 - Remote Programming. Refer to Section O - Options, for complete description.
7	TIME BASE INT/EXT Switch	This switch allows use of the internal Time Base Oscillator (A112 or A116), or use of an external 10 MHz reference generator.
8	10 MHz IN/OUT Connector	Type BNC - female connector to allow monitoring of the internal 10 MHz Time Base, or permit injection of an external 10 MHz reference signal (3 V p-p maximum).
9	TIME BASE ADJUST Control (potentiometer)	This screwdriver adjustment allows tuning of the internal 10 MHz Oven Oscillator. NOTE: This control used only with Options 03, 04, or 05 - High Stability Time Base. Refer to Section O - Options, for complete description.

SECTION 4

GENERAL THEORY OF OPERATION

4-1. GENERAL

4-2. The EIP 350D/351D Autohet Frequency Counters automatically measure and display the frequency of any CW signal from 20 Hz - 12.4 GHz (350D), or 20 Hz - 18.0 GHz (351D). In both models, this frequency coverage is obtained in three bands: 20 Hz - 300 MHz (Band I), 100 MHz - 850 MHz (Band II), and 825 MHz - 12.4/18 GHz (Band III).

4-3. Measurements in Band I are made directly with a 300 MHz counter. This band is further divided into two channels: Channel A covers the 20 Hz - 135 MHz range with an input impedance of 1 megohm shunted by 20 picofarads; Channel B covers the 10 MHz - 300 MHz range with a 50 ohm input impedance.

4-4. Band II contains a prescaler which divides the input frequency by four. It operates over the frequency range of 100 MHz - 850 MHz with 50 ohm input impedance.

4-5. Band III covers the microwave frequencies from 825 MHz to 12.4 or 18.0 GHz. In this band, an Autohet Converter translates the input frequency downward into the frequency range of the direct counter. This is accomplished by mixing the input signal with a single known harmonic of the counter Time Base oscillator, to produce a difference frequency which can be counted directly. The frequency of the known harmonic is added to the counted signal to obtain the input frequency.

4-6. Figure 4-1 shows a block diagram of the complete 350D/351D Counter. Figure 4-2 shows a block diagram of the Autohet Converter. Detailed theory and circuit descriptions of the Counter and Converter subassemblies are given in Section 9. Both the 350D and the 351D Counters are functionally identical, although differing somewhat in component selection and design.

4-7. The operation of the 350D and 351D Counters is best described by separating the instrument into two distinct functions: the direct counter, and the Autohet Converter. These two functions are interconnected in two significant areas: (1) presetting the counter to the appropriate harmonic number, and (2) counting the heterodyned difference frequency from the Converter by the direct counter.

4-8. 300 MHz DIRECT COUNTER

4-9. The measurement of frequency by the direct counter is accomplished by accumulating the number of input events (e.g: cycles of a sine wave), which occur within a precisely determined time interval. This time interval is based on the frequency of the Time Base Oscillator.

4-10. The 20 Hz - 300 MHz portion of the counter is separated physically into a number of subassemblies, designated A101 through A111 (refer to Figure 4-1, Block Diagram). The subassemblies are tied together via the Counter Interconnect Board A113. The counter is divided functionally in approximately the same manner as it is divided into subassemblies. Count Chain Boards A101, A102, and A103, operate functionally as a single unit, as do Control Boards A104 and A105. The principal interconnections between the units are shown in Figure 4-1.

4-11. Band I (20 Hz - 300 MHz) input has two operating modes. Band IA covers the 20 Hz - 135 MHz range, with 1 megohm/20 pf input impedance and 25 mV rms sensitivity. Band IA utilizes a Preamplifier (A111) containing a high input impedance amplifier, and the Band I Mode switch. Band IB (10 MHz - 300 MHz) has 50 ohm input impedance, -20 dBm sensitivity, and is routed via the Mode switch directly from the Band I input connector to the High Frequency Board (A106) input.

4-12. The Band II (100 MHz - 850 MHz) input drives the Prescaler (A109), which divides the incoming frequency by four and routes it to the High Frequency Board.

4-13. The signal input to Band III (825 MHz - 12.4/18 GHz) is translated by the Autohet Converter into the range of 25 MHz - 275 MHz, and routed to the High Frequency Board.

4-14. The outputs of these three input signal processors thus fall between 20 Hz and 300 MHz; the frequency range of the direct counter. The individual assemblies which comprise the direct counter are described in general terms below, and in detail in Section 9.

4-15. The High Frequency Board (A106) receives the input signal from one of the processors, squares the signal, and forms it into a train of constant duration pulses. This pulse train frequency is then divided by two, and sent to the Count Chain.

4-16. The Control 1 and Control 2 Boards (A104 and A105), contain circuitry to guide the counter through the steps necessary to acquire and display the input frequency. The circuits control the opening and closing of the signal gate in the High Frequency Board, and accept programming commands from the Converter, front panel controls (TEST, RESET, SAMPLE RATE), and the Remote Programming options.

4-17. The Count Chain Boards (A101, A102, and A103), accumulate the frequency from the High Frequency Board, store the accumulated information, and multiplex the stored information into a form usable by the Display

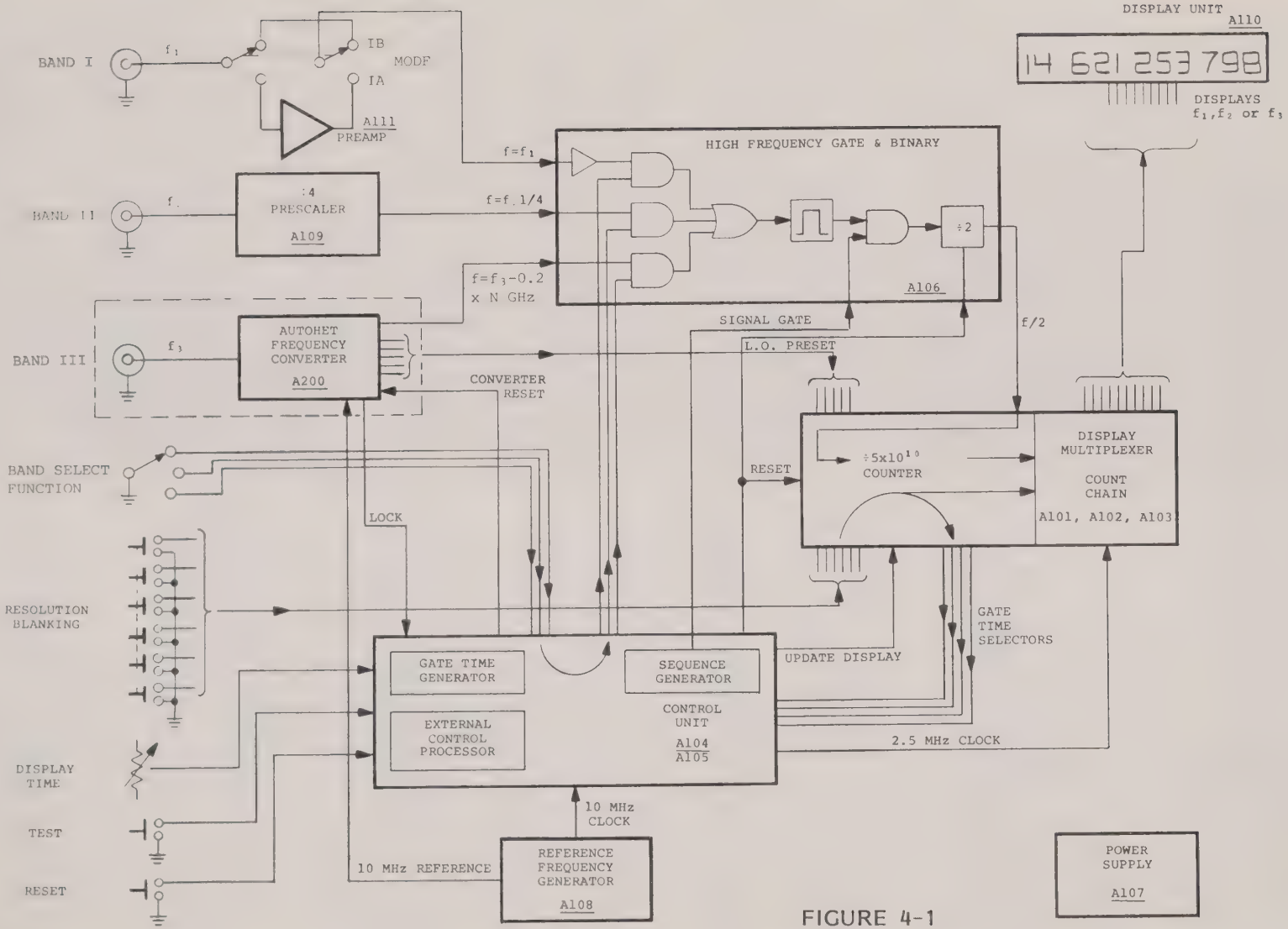


FIGURE 4-1
BLOCK DIAGRAM
350D/351D COUNTERS

Board (A110), which provides a visual display of the input frequency to the counter.

4-18. Reference Oscillator Buffer A108, produces a time base reference signal from either an internal 10 MHz oscillator, or an external 10 MHz source. All input frequencies to the counter are measured with respect to this signal.

4-19. The Power Supply (A107) provides regulated +12, -12, +5, -5.2 Vdc, and unregulated +18 Vdc. NOTE: This supply does not furnish the power for the oven stabilized Time Base Oscillators (Options 03, 04, or 05).

4-20. AUTOHET CONVERTER

4-21. The Autohet Converter is a self-contained assembly which performs the function of translating the microwave frequencies appearing at the Band III input, down into the range of the direct counter. This translation is accomplished by mixing the incoming signal with a known reference signal and then amplifying the difference frequency. The incoming frequency is then determined by counting the difference frequency and adding it to the known reference frequency. Refer to Figure 4-2, Converter Block Diagram.

4-22. The reference frequency is an integral multiple of 200 MHz which is derived from the 10 MHz Time Base Oscillator, thus maintaining the basic counter accuracy in the microwave band.

4-23. The Band III input signal passes through the 3 dB Input Attenuator (A206) and is combined in the Mixer (A205) with the reference frequency from the YIG/Comb Generator.

4-24. The YIG/Comb Generator (A207) is an integrated assembly containing a comb generator and a YIG filter. The comb generator contains a step recover diode which converts the 200 MHz sine wave input from the Source/-Amplifier (A201) into a train of narrow pulses containing all the harmonics of 200 MHz up to 12.4/18 GHz. This pulse train is then passed through a pair of YIG resonators which select the desired harmonic. The resonant frequency of the two stage filter is proportional to a magnetic field generated by passing current through a pair of coils within the structure. (A more comprehensive description of the operation of a YIG-tuned device is given later in this section.)

4-25. The Source Amplifier (A201) contains an LC oscillator operating at 200 MHz, which is phase-locked to the 10 MHz Time Base Oscillator (A116 or A112). This 200 MHz signal is amplified to produce up to one watt of output power to drive the Comb Generator section of A207.

4-26. The Mixer (A205) is an integrated microwave stripline assembly, containing a 3 dB hybrid coupler, a termination, a mixer diode, a matching network, a broadband DC return, and a bypass capacitor to separate the RF and IF signals. The Mixer produces two output signals: an IF signal with frequency equal to the difference of the reference and incoming signals, and a DC current resulting from rectification of the total power applied to the mixer diode.

4-27. Both the IF and DC signals from the Mixer enter the Video Amplifier (A204), where the IF signal is amplified, and the DC level used for gain control.

4-28. The circuitry required to control the Autohet Converter is located on two Converter Control Boards (A202 and A203). Their function is to set the YIG Filter within the YIG/Comb Generator (A207) to the correct harmonics of 200 MHz, and to provide both the IF frequency and the harmonic information to the direct counter.

4-29. To accomplish this, the YIG Filter passband is continuously tuned over the operating range until an appropriate signal is received from the Video Amplifier. The sweep is then stopped so the YIG Filter passband is centered on the desired harmonic. Converter Control 1 (A203) performs all the signal processing and provides digital commands to Converter Control 2 (A202) which contains the Digital to Analog Converters and the current driver necessary to tune the YIG Filter. A detailed operational sequence is described in Section 9 in the Converter Control 1 description (Figure 9-17).

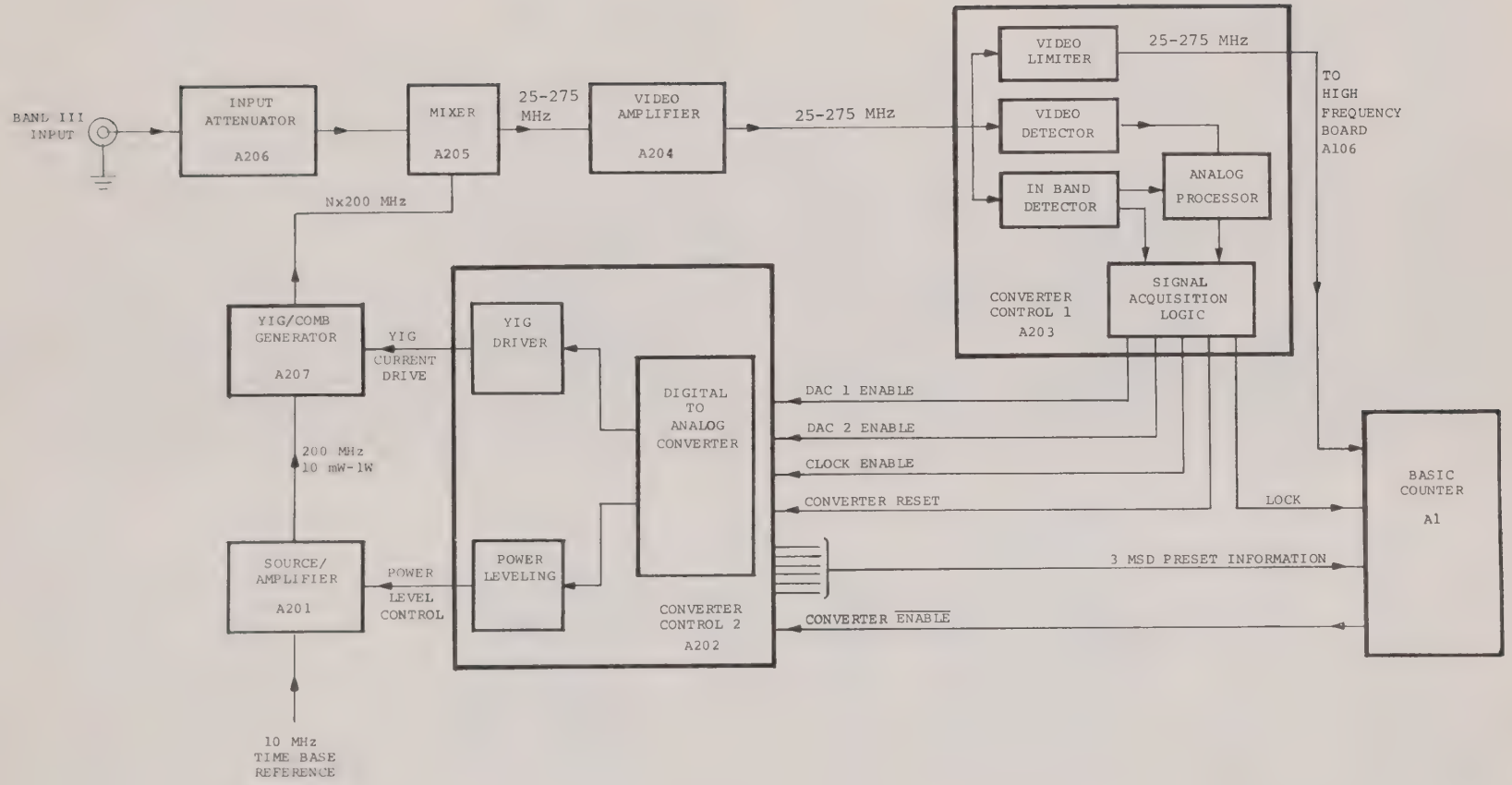


FIGURE 4-2
BLOCK DIAGRAM
AUTOHET CONVERTER
350D/351D COUNTERS

AN INTRODUCTION TO YIG FILTERS

Highly polished spheres of single crystal YIG (yttrium-iron-garnet), have a property called ferrimagnetic resonance. Basically, the ferrimagnetic resonance phenomenon can be explained in terms of spinning electrons creating a net magnetic moment in each molecule of a YIG crystal (see Figure A). Viewing the material macroscopically, there is no net effect because the magnetic dipoles associated with each molecule are randomly oriented (see Figure B). The application of an external magnetic biasing field, H_{DC}, causes the magnetic dipoles to be aligned in the direction of the biasing field (see Figure C).

An RF field can be used to create an orthogonal magnetic force. If the frequency of the RF field coincides with the natural precession frequency, there is a strong interaction called ferrimagnetic resonance (Figure D).

Figure E shows the basic elements of a YIG bandpass filter. The filter consists of a YIG sphere at the center of two loops. The two loops are perpendicular to each other and to the dc biasing field, H_{DC}. One loop carries the RF input and the other the RF output. When the RF signal frequency is the same as the natural precession frequency of the YIG, there is strong coupling between the input and output loops. Thus RF can only pass through the YIG filter at resonance. The resonant frequency is a linear function of the magnetic biasing field, H_{DC}. Generally, H_{DC} is provided by locating the YIG spheres between the poles of an electromagnet, and tuned by varying the current to the magnetic coils.

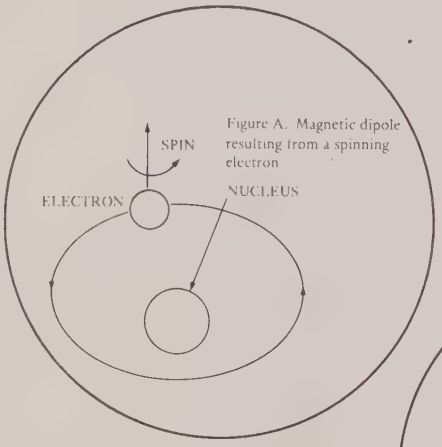


Figure A. Magnetic dipole resulting from a spinning electron

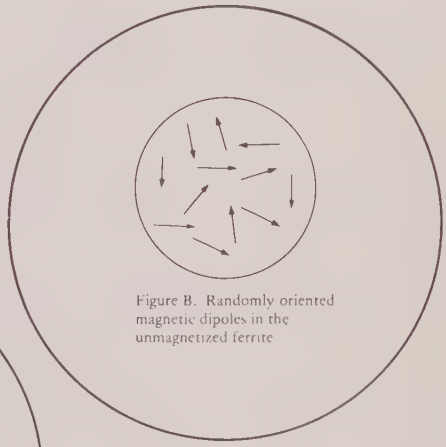


Figure B. Randomly oriented magnetic dipoles in the unmagnetized ferrite

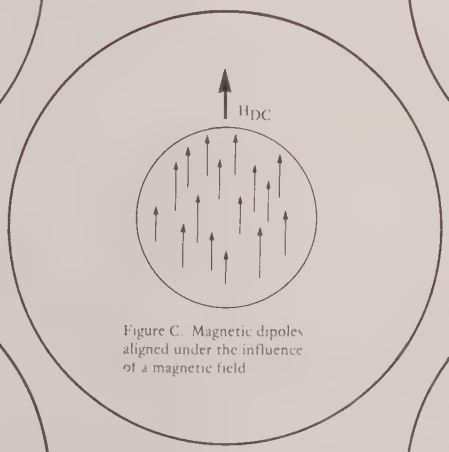


Figure C. Magnetic dipoles aligned under the influence of a magnetic field

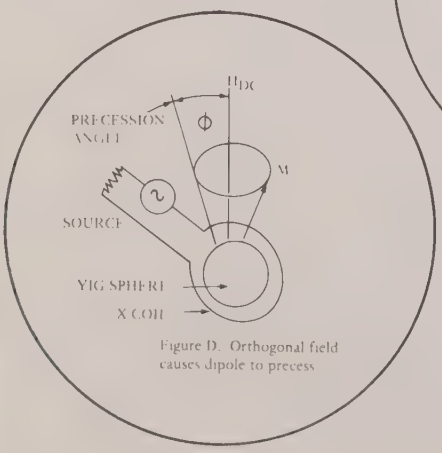


Figure D. Orthogonal field causes dipole to precess

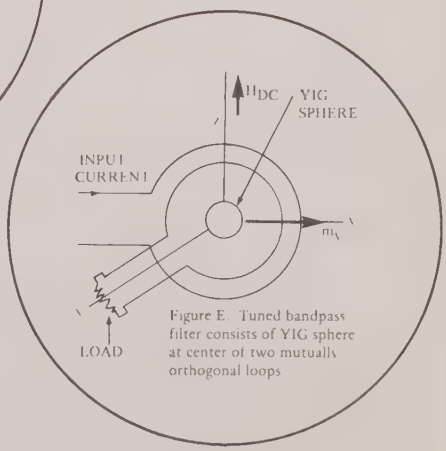


Figure E. Tuned bandpass filter consists of YIG sphere at center of two mutually orthogonal loops

SECTION 5

MAINTENANCE & SERVICE

5-1. GENERAL

5-2. This section provides instructions, procedures, and information necessary to maintain, troubleshoot, and repair the 350D/351D Autohet Counter.

5-3. FUSE REPLACEMENT

5-4. The counter uses one fuse, located on the rear panel. For proper operation, use only the fuse specified below; do not increase fuse rating or change fuse type. Set 115/230 slide switch on rear panel to match nominal power line voltage.

For 115 VAC operation: use a 1.5A, Slow-Blow, 3AB/MDX type fuse.

For 230 VAC operation: use a 0.75A, Slow-Blow, 3AB/MDL type fuse.

5-5. AIR CIRCULATION

5-6. During operation of the counter, the internal fan draws in cooling air through the vents in the enclosure. If these vents are blocked, the temperature inside the enclosure may rise to the point where counter stability is reduced, and component life shortened.

5-7. COUNTER SERVICING

5-8. Recommended Service Procedures:

a. To remove plug-in PC Boards: Ease board out of socket by lifting up on board handles. Remove carefully to avoid placing strain on any connecting cables.

b. To unplug flat ribbon cables: Turn off power to counter. Use an IC Extractor Tool (EIP Part 5000094 or equivalent) to unplug connector.

c. To remove PCB socket locating key: Key must be turned 90° before removal from or re-installation into socket, to avoid contact damage. Use long-nose pliers for removal or insertion.

d. A Troubleshooting Kit (EIP Part 2000005) is available to facilitate adjustments and repairs of the counter. Contents include PCB Extender Cards, IC Removal Tool, Summing Amplifier, adapter cables and connectors.

e. Internal cable and harness routing is shown both on a label attached to the top cover of the counter, and in Figure 9-2.

f. Circuit descriptions of PC Board and modular assemblies are shown on the same pages as the related schematic diagram and component locator in Section 9.

g. Troubleshooting Trees shown later in this section are intended only as a guide, and do not describe every possible failure situation. To speed troubleshooting of a board: replace the board with a known good one.

h. A listing of recommended test equipment for servicing, calibration, and performance testing, is given in Table 5-1. Other equipment may be used provided performance equals or exceeds that listed.

i. A Schematic Diagram of a Summing Amplifier used in certain counter tests, is shown in Figure 5-1. This unit may be constructed by the user, or may be purchased directly from EIP (Part Number 2010050).

5-9. Servicing Precautions

a. The Video Amplifier (A204) and the Source/Amplifier (A201) should be replaced rather than being serviced in the field, due to the specialized test equipment and procedures required for recalibration.

b. If Converter Control 2 (A202) is repaired either at EIP or in the field, recalibration in its associated counter will be required for proper counter operation.

> CAUTION
>
> DO NOT ATTEMPT REPAIR OR DISASSEMBLY OF THE FOLLOWING COMPONENTS: YIG/COMB GENERATOR (A207), MIXER (A205), INPUT ATTENUATOR (A206), OR TIME BASE OSCILLATOR (TCXO OR OVEN OPTION).

5-10. FACTORY SERVICE

5-11. If the counter is to be returned to EIP for service or repair, BE SURE TO INCLUDE THE FOLLOWING INFORMATION WITH THE SHIPMENT: *

a. Name and address of owner.

b. Model and complete serial number of counter.

c. A COMPLETE description of trouble (e.g: under

EQUIPMENT DESCRIPTION	MFR.	MODEL	Section 5 - Service	Section 6 - Calibration	Section 7 - Performance
Signal Source: (1) 20 Hz - 10 MHz	HP	651B	x		x
(2) 10 MHz - 1 GHz	Wavetek	2001B	x	x	x
(3) 1 GHz - 12.4/18 GHz	S-D	521-series	x	x	x
Oscilloscope (Main Frame)	HP	180C	x	x	
Dual Channel Ampl. (Plug-In)	HP	1801A	x	x	
Delayed Time Base (Plug-In)	HP	1821A	x	x	
Digital Voltmeter (4½ digit)	Dana	4800	x	x	
Power Meter	HP	432B	x	x	x
Thermistor Mount (10 MHz-18 GHz)	HP	8478	x	x	x
Frequency Standard	HP	105A		x	
VLF Comparator	HP	117A		x	
Summing Amplifier *	EIP	2010050*	x	x	
Variable 115 Vac Source	Staco	3PN501			x
Extender Card	EIP	2020021	x	x	
Adapter Cable (SMC to BNC)	EIP	2040015	x	x	
Misc. attenuators, adapters and cables			x	x	x

* See Figure 5-1.

TABLE 5-1. RECOMMENDED TEST EQUIPMENT

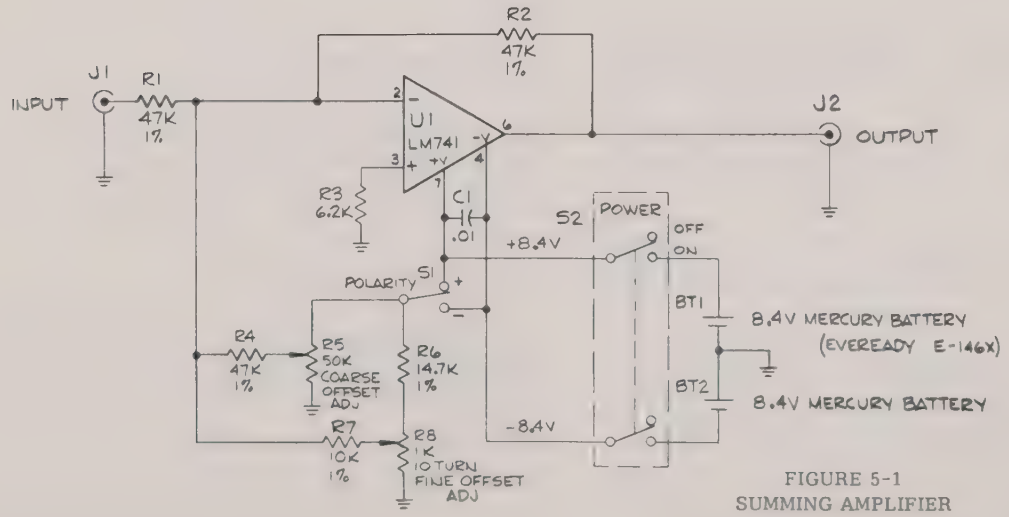


FIGURE 5-1
SUMMING AMPLIFIER

what conditions did trouble occur? What was the signal level? What associated equipment was attached or connected to the counter? Did that equipment fail too?)*

d. Name and telephone number of someone familiar with the problem, who may be contacted by EIP for any further information if necessary.

e. Shipping address to which counter is to be returned; include any special shipping instructions.

f. Pack the counter as follows:

(1) Wrap the counter in plastic or heavy kraft paper, and repack in the original shipping container (if still available) using the original packing material.

(2) If the original container and packing material are no longer available, use a heavy (275 lb. test) double-walled carton, with approximately 4" of suitable packing material between the inner and outer walls, with additional packing material as required between the counter and the inner carton. Seal with strong filamentary tape or strapping.

(3) Mark the shipping container to indicate that it contains fragile electronic instruments. Ship to EIP at address shown on title page of this manual.

* A COUNTER REPAIR AND RETURN FORM IS BOUND INTO THE BACK OF THIS MANUAL. IF THE FORM IS MISSING, PLEASE SUPPLY THE INFORMATION REQUESTED IN THE ABOVE PARAGRAPH.

5-12. TROUBLESHOOTING

5-13. MALFUNCTION AT TURN ON

5-14. If the counter fails to turn on (no display, no fan, etc.), make the following checks:

a. 115/230 switch at proper setting.

b. Power cord plugged into counter and into AC power source.

c. Correct AC power available at source.

d. Counter fuse good.

e. POWER switch in "On" position (button depressed and green indicator showing).

f. PC Boards and connectors are properly engaged.

g. Counter power supply voltages correct (measured on Counter Interconnect PC Board A113).

5-15. FAILURE TO INDICATE ALL ZEROS

5-16. If counter turns on, but fails to indicate all zeros with no applied signal, CHECK THAT:

a. No RESOLUTION switches are depressed.

b. INT/EXT switch is set to INT.

c. PC Boards and connectors are properly engaged.

d. Counter Power Supply (A107) voltages correct.

e. Perform Visual Display Test by pressing TEST and RESET switches simultaneously; display should show "8" in all decade positions.

f. If counter fails the Visual Display Test, refer to Troubleshooting Tree - Figure 5-2. If counter displays all eights but a digit is missing, refer to Figure 5-3. If the display does not show all zeros when it should, refer to Figure 5-4.

5-17. MALFUNCTION IN SELF TEST

5-18. If counter turns on, but fails to indicate a reading of 10 000 000 (10 MHz) in the TEST mode, CHECK THAT:

a. Counter indicates all zeros with no applied signal.

b. PC Boards and connectors are properly engaged.

c. Counter Power Supply (A107) voltages correct.

d. Counter passes Visual Display Test (para. 5-16).

e. Refer to Figure 5-5.

5-19. MALFUNCTION IN BAND IB (10 MHz to 300 MHz)

5-20. If counter fails to read frequency correctly, CHECK THAT:

a. BAND SELECT switch is fully left in the Band I position, and the Band I Mode Switch is in the 10 MHz - 300 MHz position.

b. A signal is applied to the Band I input connector. The signal level and frequency should be as specified for Band IB.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Refer to Figure 5-6.

5-21. MALFUNCTION IN BAND IA
(20 Hz to 135 MHz)

5-22. If counter fails to read frequency correctly, CHECK THAT:

a. BAND SELECT switch is fully left in the Band I position, and the Band I Mode switch is in the 20 Hz - 135 MHz position.

b. A signal is applied to the Band I input connector. The signal level and frequency should be as specified for Band IA.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Counter operates properly in Band IB.

g. Refer to Figure 5-7.

5-23. MALFUNCTION IN BAND II
(100 MHz to 850 MHz)

5-24. If counter fails to read frequency correctly, CHECK THAT:

a. BAND SELECT switch is in the center (Band II) position.

b. A signal is applied to the Band II input connector. The signal level and frequency should be as specified for Band II.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Prescaler PC Board (A109) connector and co-ax cables properly engaged.

g. Counter operates properly in Band IB.

h. Refer to Figure 5-8.

5-25. MALFUNCTION IN BAND III
(825 MHz to 12.4/18 GHz)

5-26. If counter fails to read frequency correctly, CHECK THAT:

a. BAND SELECT switch is in the fully right (Band III) position.

b. A signal is applied to the Band III input connector. The signal level and frequency should be as specified for Band III.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Counter operates properly in Bands I and II.

g. Converter Control (A202 and A203) PC Board connectors and co-ax cables are properly engaged.

h. Refer to Figure 5-9.

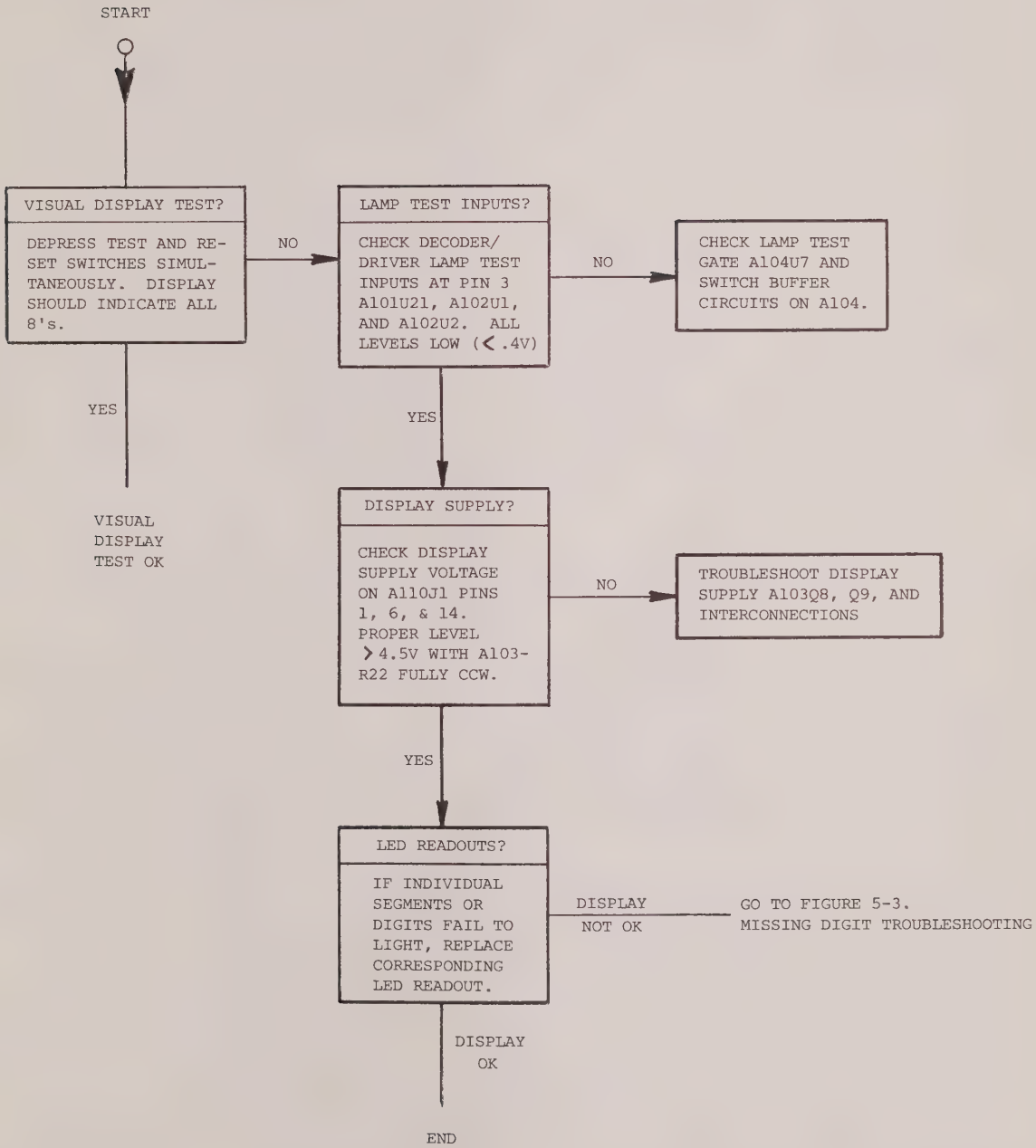


FIGURE 5-2
VISUAL DISPLAY TEST
TROUBLESHOOTING TREE

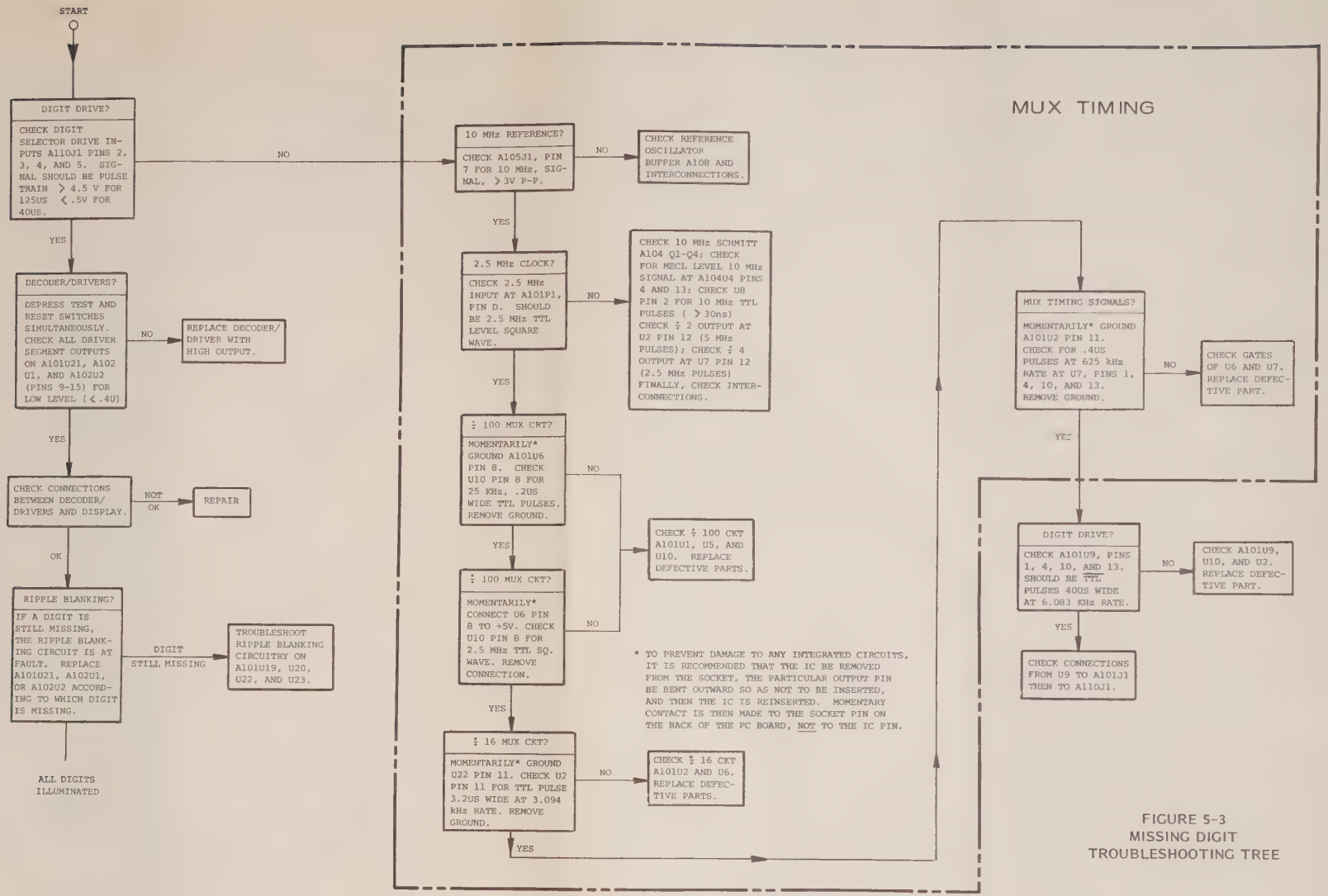

START
DIGIT DRIVE?
CHECK DIGIT SELECTOR DRIVE INPUTS A110J1 PINS 2, 3, 4, AND 5. SIGNAL SHOULD BE PULSE TRAIN > 4.5 V FOR 125US < .5V FOR 40US.
NO
YES
DECODER/DRIVERS?
DEPRESS TEST AND RESET SWITCHES SIMULTANEOUSLY. CHECK ALL DRIVER SEGMENT OUTPUTS ON A101U21, A102U1, AND A102U2 (PINS 9-15) FOR LOW LEVEL (< .4U)
NO
REPLACE DECODER/DRIVER WITH HIGH OUTPUT.
YES
CHECK CONNECTIONS BETWEEN DECODER/DRIVERS AND DISPLAY.
NOT OK
REPAIR
OK
RIPPLE BLANKING?
IF A DIGIT IS STILL MISSING, THE RIPPLE BLANKING CIRCUIT IS AT FAULT. REPLACE A101U21, A102U1, OR A102U2 ACCORDING TO WHICH DIGIT IS MISSING.
DIGIT STILL MISSING
TROUBLESHOOT RIPPLE BLANKING CIRCUITRY ON A101U19, U20, U22, AND U23.
ALL DIGITS ILLUMINATED
10 MHz REFERENCE?
CHECK A105J1, PIN 7 FOR 10 MHz, SIGNAL, > 3V P-P.
NO
CHECK REFERENCE OSCILLATOR BUFFER A108 AND INTERCONNECTIONS.
YES
2.5 MHz CLOCK?
CHECK 2.5 MHz INPUT AT A101P1, PIN D. SHOULD BE 2.5 MHz TTL LEVEL SQUARE WAVE.
NO
CHECK 10 MHz SCHMITT A104 Q1-Q4; CHECK FOR MECL LEVEL 10 MHz SIGNAL AT A104U4 PINS 4 AND 13; CHECK U8 PIN 2 FOR 10 MHz TTL PULSES (> 30ns) CHECK ÷ 2 OUTPUT AT U2 PIN 12 (5 MHz PULSES); CHECK ÷ 4 OUTPUT AT U7 PIN 12 (2.5 MHz PULSES) FINALLY, CHECK INTERCONNECTIONS.
YES
÷ 100 MUX CRT?
MOMENTARILY* GROUND A101U6 PIN 8. CHECK U10 PIN 8 FOR 25 KHz, .2US WIDE TTL PULSES. REMOVE GROUND.
NO
YES
÷ 100 MUX CKT?
MOMENTARILY* CONNECT U6 PIN 8 TO +5V. CHECK U10 PIN 8 FOR 2.5 MHz TTL SQ. WAVE. REMOVE CONNECTION.
NO
CHECK ÷ 100 CKT A101U1, U5, AND U10. REPLACE DEFECTIVE PARTS.
YES
÷ 16 MUX CKT?
MOMENTARILY* GROUND U22 PIN 11. CHECK U2 PIN 11 FOR TTL PULSE 3.2US WIDE AT 3.094 kHz RATE. REMOVE GROUND.
NO
CHECK ÷ 16 CKT A101U2 AND U6. REPLACE DEFECTIVE PARTS.
YES
* TO PREVENT DAMAGE TO ANY INTEGRATED CIRCUITS, IT IS RECOMMENDED THAT THE IC BE REMOVED FROM THE SOCKET, THE PARTICULAR OUTPUT PIN BE BENT OUTWARD SO AS NOT TO BE INSERTED, AND THEN THE IC IS REINSERTED. MOMENTARY CONTACT IS THEN MADE TO THE SOCKET PIN ON THE BACK OF THE PC BOARD, NOT TO THE IC PIN.
MUX TIMING
MUX TIMING SIGNALS?
MOMENTARILY* GROUND A101U2 PIN 11. CHECK FOR .4US PULSES AT 625 kHz RATE AT U7, PINS 1, 4, 10, AND 13. REMOVE GROUND.
NO
CHECK GATES OF U6 AND U7. REPLACE DEFECTIVE PART.
YES
DIGIT DRIVE?
CHECK A101U9, PINS 1, 4, 10, AND 13. SHOULD BE TTL PULSES 400S WIDE AT 6.083 KHz RATE.
NO
CHECK A101U9, U10, AND U2. REPLACE DEFECTIVE PART.
YES
CHECK CONNECTIONS FROM U9 TO A101J1 THEN TO A110J1.

FIGURE 5-3
MISSING DIGIT
TROUBLESHOOTING TREE

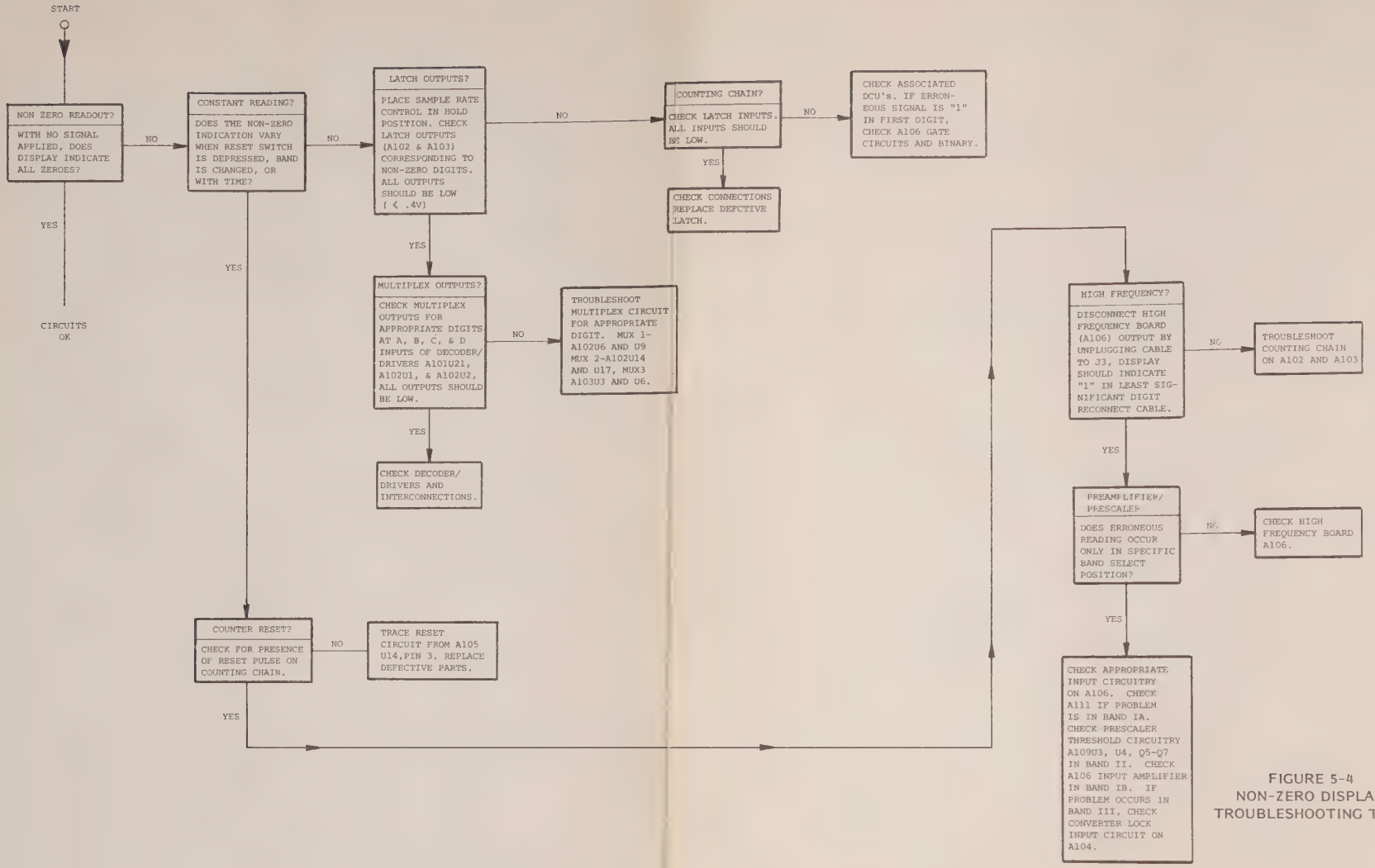

START
NON ZERO READOUT?
WITH NO SIGNAL APPLIED, DOES DISPLAY INDICATE ALL ZEROES?
NO
YES
CIRCUITS OK
CONSTANT READING?
DOES THE NON-ZERO INDICATION VARY WHEN RESET SWITCH IS DEPRESSED, BAND IS CHANGED, OR WITH TIME?
NO
YES
LATCH OUTPUTS?
PLACE SAMPLE RATE CONTROL IN HOLD POSITION. CHECK LATCH OUTPUTS (A102 & A103) CORRESPONDING TO NON-ZERO DIGITS. ALL OUTPUTS SHOULD BE LOW (< .4V)
NO
YES
COUNTING CHAIN?
CHECK LATCH INPUTS. ALL INPUTS SHOULD BE LOW.
NO
YES
CHECK ASSOCIATED DCU's. IF ERRONEOUS SIGNAL IS "1" IN FIRST DIGIT, CHECK A106 GATE CIRCUITS AND BINARY.
CHECK CONNECTIONS REPLACE DEFCTIVE LATCH.
MULTIPLEX OUTPUTS?
CHECK MULTIPLEX OUTPUTS FOR APPROPRIATE DIGITS AT A, B, C, & D INPUTS OF DECODER/DRIVERS A101U21, A102U1, & A102U2, ALL OUTPUTS SHOULD BE LOW.
NO
YES
TROUBLESHOOT MULTIPLEX CIRCUIT FOR APPROPRIATE DIGIT. MUX 1-A102U6 AND U9 MUX 2-A102U14 AND U17, MUX3 A103U3 AND U6.
CHECK DECODER/DRIVERS AND INTERCONNECTIONS.
COUNTER RESET?
CHECK FOR PRESENCE OF RESET PULSE ON COUNTING CHAIN.
NO
YES
TRACE RESET CIRCUIT FROM A105 U14,PIN 3. REPLACE DEFECTIVE PARTS.
HIGH FREQUENCY?
DISCONNECT HIGH FREQUENCY BOARD (A106) OUTPUT BY UNPLUGGING CABLE TO J3, DISPLAY SHOULD INDICATE "1" IN LEAST SIGNIFICANT DIGIT RECONNECT CABLE.
NO
YES
TROUBLESHOOT COUNTING CHAIN ON A102 AND A103
PREAMPLIFIER/PRESCALER
DOES ERRONEOUS READING OCCUR ONLY IN SPECIFIC BAND SELECT POSITION?
NO
YES
CHECK HIGH FREQUENCY BOARD A106.
CHECK APPROPRIATE INPUT CIRCUITRY ON A106. CHECK A111 IF PROBLEM IS IN BAND IA. CHECK PRESCALER THRESHOLD CIRCUITRY A109U3, U4, Q5-Q7 IN BAND II. CHECK A106 INPUT AMPLIFIER IN BAND IB. IF PROBLEM OCCURS IN BAND III, CHECK CONVERTER LOCK INPUT CIRCUIT ON A104.

FIGURE 5-4
NON-ZERO DISPLAY
TROUBLESHOOTING TREE

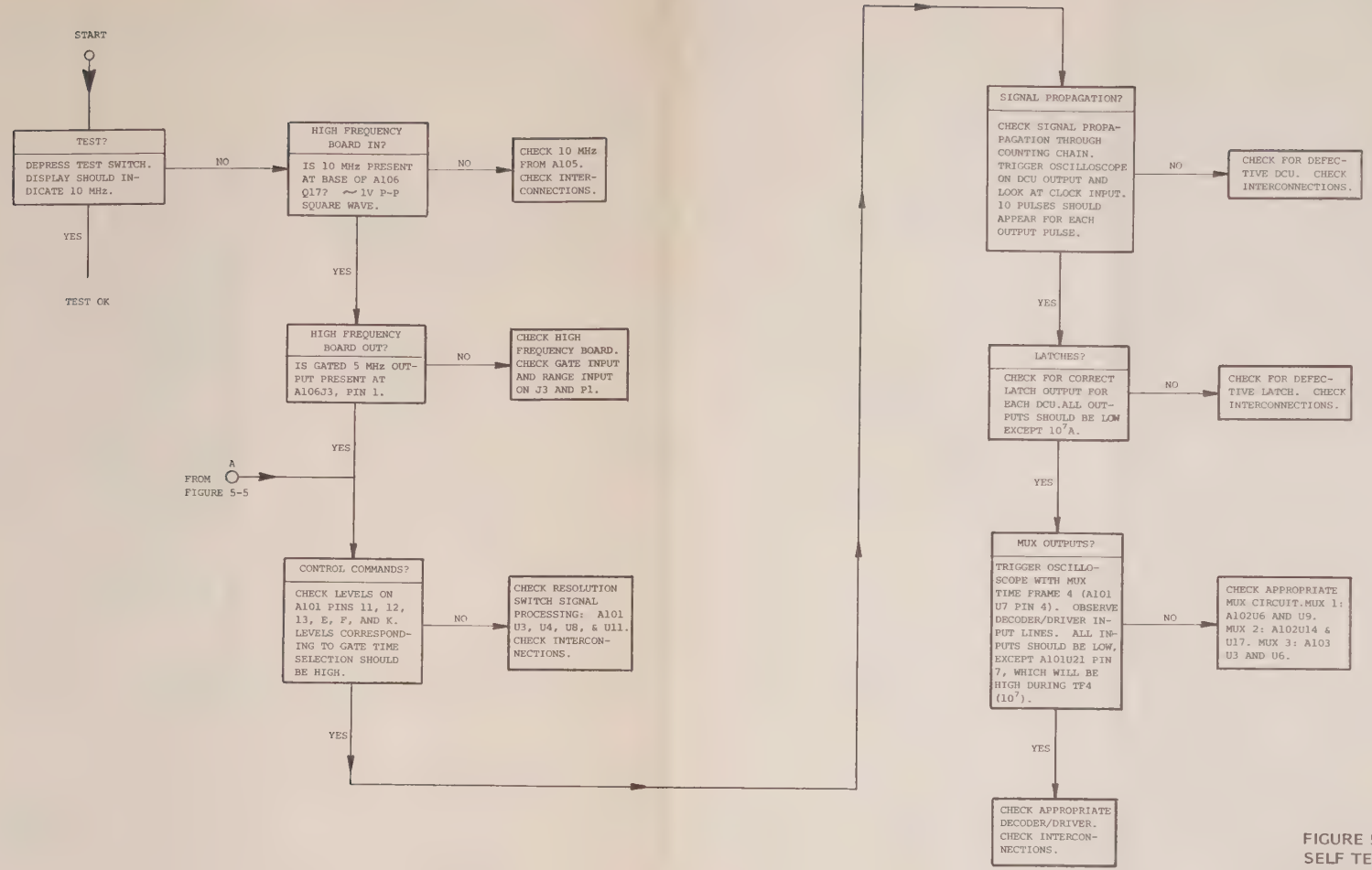
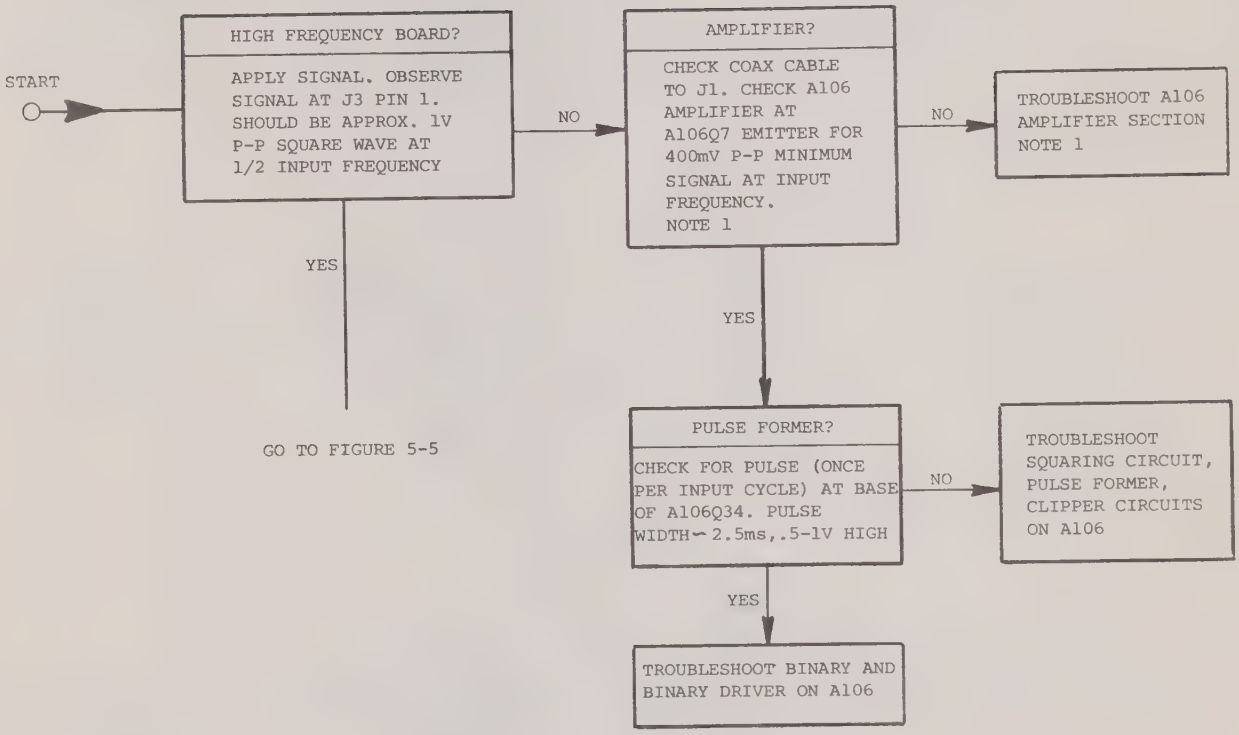

START
TEST?
DEPRESS TEST SWITCH. DISPLAY SHOULD INDICATE 10 MHz.
NO
YES
TEST OK
HIGH FREQUENCY BOARD IN?
IS 10 MHz PRESENT AT BASE OF A106 Q17? ~1V P-P SQUARE WAVE.
NO
CHECK 10 MHz FROM A105. CHECK INTERCONNECTIONS.
YES
HIGH FREQUENCY BOARD OUT?
IS GATED 5 MHz OUTPUT PRESENT AT A106J3, PIN 1.
NO
CHECK HIGH FREQUENCY BOARD. CHECK GATE INPUT AND RANGE INPUT ON J3 AND P1.
YES
A
FROM FIGURE 5-5
CONTROL COMMANDS?
CHECK LEVELS ON A101 PINS 11, 12, 13, E, F, AND K. LEVELS CORRESPONDING TO GATE TIME SELECTION SHOULD BE HIGH.
NO
CHECK RESOLUTION SWITCH SIGNAL PROCESSING: A101 U3, U4, U8, & U11. CHECK INTERCONNECTIONS.
YES
SIGNAL PROPAGATION?
CHECK SIGNAL PROPAGATION THROUGH COUNTING CHAIN. TRIGGER OSCILLOSCOPE ON DCU OUTPUT AND LOOK AT CLOCK INPUT. 10 PULSES SHOULD APPEAR FOR EACH OUTPUT PULSE.
NO
CHECK FOR DEFECTIVE DCU. CHECK INTERCONNECTIONS.
YES
LATCHES?
CHECK FOR CORRECT LATCH OUTPUT FOR EACH DCU.ALL OUTPUTS SHOULD BE LOW EXCEPT 10^7A.
NO
CHECK FOR DEFECTIVE LATCH. CHECK INTERCONNECTIONS.
YES
MUX OUTPUTS?
TRIGGER OSCILLOSCOPE WITH MUX TIME FRAME 4 (A101 U7 PIN 4). OBSERVE DECODER/DRIVER INPUT LINES. ALL INPUTS SHOULD BE LOW, EXCEPT A101U21 PIN 7, WHICH WILL BE HIGH DURING TF4 (10^7).
NO
CHECK APPROPRIATE MUX CIRCUIT.MUX 1: A102U6 AND U9. MUX 2: A102U14 & U17. MUX 3: A103 U3 AND U6.
YES
CHECK APPROPRIATE DECODER/DRIVER. CHECK INTERCONNECTIONS.

FIGURE 5-5
SELF TEST
TROUBLESHOOTING TREE


START
HIGH FREQUENCY BOARD?
APPLY SIGNAL. OBSERVE SIGNAL AT J3 PIN 1. SHOULD BE APPROX. 1V P-P SQUARE WAVE AT 1/2 INPUT FREQUENCY
NO
AMPLIFIER?
CHECK COAX CABLE TO J1. CHECK A106 AMPLIFIER AT A106Q7 EMITTER FOR 400mV P-P MINIMUM SIGNAL AT INPUT FREQUENCY. NOTE 1
NO
TROUBLESHOOT A106 AMPLIFIER SECTION NOTE 1
YES
GO TO FIGURE 5-5
YES
PULSE FORMER?
CHECK FOR PULSE (ONCE PER INPUT CYCLE) AT BASE OF A106Q34. PULSE WIDTH ~ 2.5ms, .5-1V HIGH
NO
TROUBLESHOOT SQUARING CIRCUIT, PULSE FORMER, CLIPPER CIRCUITS ON A106
YES
TROUBLESHOOT BINARY AND BINARY DRIVER ON A106

NOTE 1:
TROUBLESHOOTING OF A106 REQUIRES THE USE OF A SAMPLING OSCILLOSCOPE WITH 1 GHz OR GREATER BANDWIDTH. CARE MUST BE EXERCISED TO LOAD CIRCUIT JUNCTION LIGHTLY. MAXIMUM PROBE CAPACITANCE 1PF. MINIMUM RESISTANCE 500 OHMS.

FIGURE 5-6
BAND IB
TROUBLESHOOTING TREE

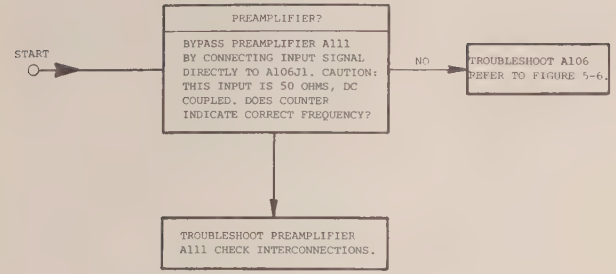
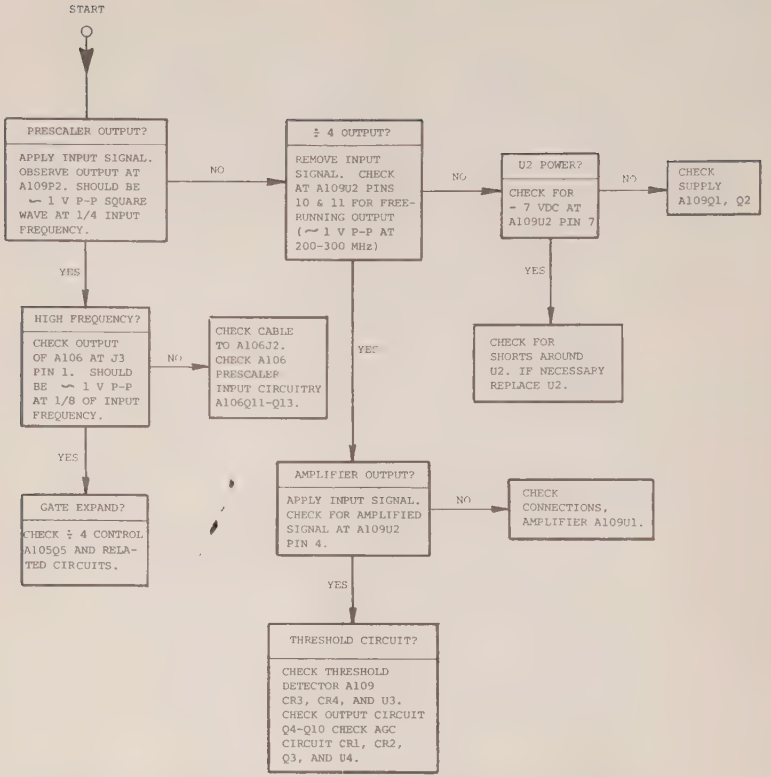
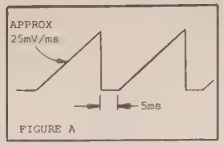

START
PREAMPLIFIER?
BYPASS PREAMPLIFIER A111 BY CONNECTING INPUT SIGNAL DIRECTLY TO A106J1. CAUTION: THIS INPUT IS 50 OHMS, DC COUPLED. DOES COUNTER INDICATE CORRECT FREQUENCY?
NO
TROUBLESHOOT A106 REFER TO FIGURE 5-6.
TROUBLESHOOT PREAMPLIFIER A111 CHECK INTERCONNECTIONS.

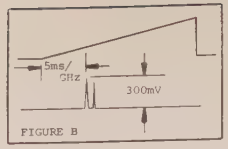
FIGURE 5-7
BAND IA
TROUBLESHOOTING TREE


START
PRESCALER OUTPUT?
APPLY INPUT SIGNAL. OBSERVE OUTPUT AT A109P2. SHOULD BE ∽ 1 V P-P SQUARE WAVE AT 1/4 INPUT FREQUENCY.
NO
÷ 4 OUTPUT?
REMOVE INPUT SIGNAL. CHECK AT A109U2 PINS 10 & 11 FOR FREE-RUNNING OUTPUT (∽ 1 V P-P AT 200-300 MHz)
NO
U2 POWER?
CHECK FOR - 7 VDC AT A109U2 PIN 7
NO
CHECK SUPPLY A109Q1, Q2
YES
YES
HIGH FREQUENCY?
CHECK OUTPUT OF A106 AT J3 PIN 1. SHOULD BE ∽ 1 V P-P AT 1/8 OF INPUT FREQUENCY.
NO
CHECK CABLE TO A106J2. CHECK A106 PRESCALER INPUT CIRCUITRY A106Q11-Q13.
YES
CHECK FOR SHORTS AROUND U2. IF NECESSARY REPLACE U2.
YES
GATE EXPAND?
CHECK ÷ 4 CONTROL A105Q5 AND RELATED CIRCUITS.
AMPLIFIER OUTPUT?
APPLY INPUT SIGNAL. CHECK FOR AMPLIFIED SIGNAL AT A109U2 PIN 4.
NO
CHECK CONNECTIONS, AMPLIFIER A109U1.
YES
THRESHOLD CIRCUIT?
CHECK THRESHOLD DETECTOR A109 CR3, CR4, AND U3. CHECK OUTPUT CIRCUIT Q4-Q10 CHECK AGC CIRCUIT CR1, CR2, Q3, AND U4.

NOTE 1:
TROUBLESHOOTING OF A106 REQUIRES THE USE OF A SAMPLING OSCILLOSCOPE WITH 1 GHz OR GREATER BANDWIDTH. CARE MUST BE EXERCIZED TO LOAD CIRCUIT JUNCTION LIGHTLY. MAXIMUM PROBE CAPACITANCE 1PF. MINIMUM RESISTANCE 500 OHMS.

FIGURE 5-8
BAND II
TROUBLESHOOTING TREE





START

PHASE LOCK?

PLACE BAND SELECT SWITCH TO BAND I. DISCONNECT CABLE FROM A201J1 AND CONNECT J1 THROUGH A 20 DB ATTENUATOR TO BAND I INPUT. COUNTER SHOULD READ 200 000 000 + 1.

CAUTION: OMISSION OF ATTENUATOR MAY CAUSE EXTENSIVE DAMAGE TO COUNTER. WITH BAND SELECT SWITCH IN BAND I POSITION, J1 OUTPUT IS APPROX. +10 dBm. IN BAND III POSITION, OUTPUT IS UP TO 1W.

NO → CHECK ALL INPUTS TO SOURCE/AMPLIFIER A201. TROUBLESHOOT OR REPLACE A201.

YES

YIG PRESET?

REMOVE CABLE TO A106J4. DISPLAYED FREQUENCY IS YIG PRESET. SHOULD BE BELOW INPUT FREQUENCY BY 25-275 MHz

NO → CHECK DAC 1 OUTPUTS ON A202. CHECK 3MSD DCU's ON A102. CHECK CONNECTIONS. CHECK YIG OFFSET AND SLOPE CALIBRATIONS. REFER TO SECTION 6.

YES

CHECK YIG DELAY CALIBRATION
CHECK VIDEO LIMITER A203Q3-Q5.
CHECK A106 INPUT CIRCUITRY Q14-Q16.

YES

CONVERTER LOCK?

RECONNECT CONVERTER. SET BAND SELECT SWITCH TO BAND III. APPLY INPUT SIGNAL. SEARCH INDICATOR SHOULD GO OUT.

NO

RAMP

GROUND A203TP2. CONNECT OSCILLOSCOPE TO NEGATIVE TERMINAL OF "I" TUNING COIL A207 (-). PRESENTATION SHOULD BE SIMILAR TO FIG. A.

NO → ENABLE COMMANDS?

CHECK A202P1, PIN E FOR TTL HIGH; PIN 5 FOR TTL LOW.

NO → CHECK A201 U11, U13, U16.

YES → CHECK ON A202:
a. DAC CLOCK
b. DAC #1
c. YIG DRIVER

YES

YES

DETECTED COMB LINES?

REMOVE INPUT SIGNAL. AC COUPLE OSCILLOSCOPE AND SET TO 100 MV/DIV. MONITOR A204J3. COMB LINES SIMILAR TO FIG. 6-3 SHOULD BE OBSERVED.

SOME LINES WEAK OR MISSING → PERFORM CALIBRATION ACCORDING TO PARA. 6-7d.

ALL LINES WEAK OR MISSING → GO TO MIXER TEST FIGURE 5-9B

YES

VIDEO DETECTOR?

GROUND A203TP2. APPLY INPUT SIGNAL. CONNECT OSCILLOSCOPE CHANNEL A TO A207(-)(RAMP), AND CH. B TO A203TP7 (VIDEO DETECTOR). DISPLAY SHOULD APPEAR AS IN FIGURE B.

NO → CHECK VIDEO DETECTOR CIRCUIT A203Q2, CR8, AND U3. IF OK, REPLACE VIDEO AMPLIFIER A204.

YES

A203 CONTROL CIRCUITS?

MOVE GROUND FROM A203 TP2 TO TP4. APPLY INPUT SIGNAL. LOOK FOR SIGNALS AS SHOWN IN FIGURE 9-17C.

MISSING SIGNAL → TROUBLESHOOT APPROPRIATE SECTION OF A203.

ALL PRESENT

A202 DAC CIRCUITS?

CHECK A202 DAC 2. PERFORM ALL CALIBRATION STEPS IN SECTION 6.

NOTES:
1. THE FOLLOWING ASSEMBLIES ARE FIELD REPLACEABLE ONLY:
   a. YIG/COMB GENERATOR A207.
   b. MIXER A205.
   c. ATTENUATOR A206.
2. THE FOLLOWING REQUIRE SPECIAL EQUIPMENT AND ARE DIFFICULT TO REPAIR IN THE FIELD: (REPLACEMENT IS RECOMMENDED)
   a. SOURCE/AMPLIFIER A201.
   b. VIDEO AMPLIFIER A204.

FIGURE 5-9A
BAND III
TROUBLESHOOTING TREE

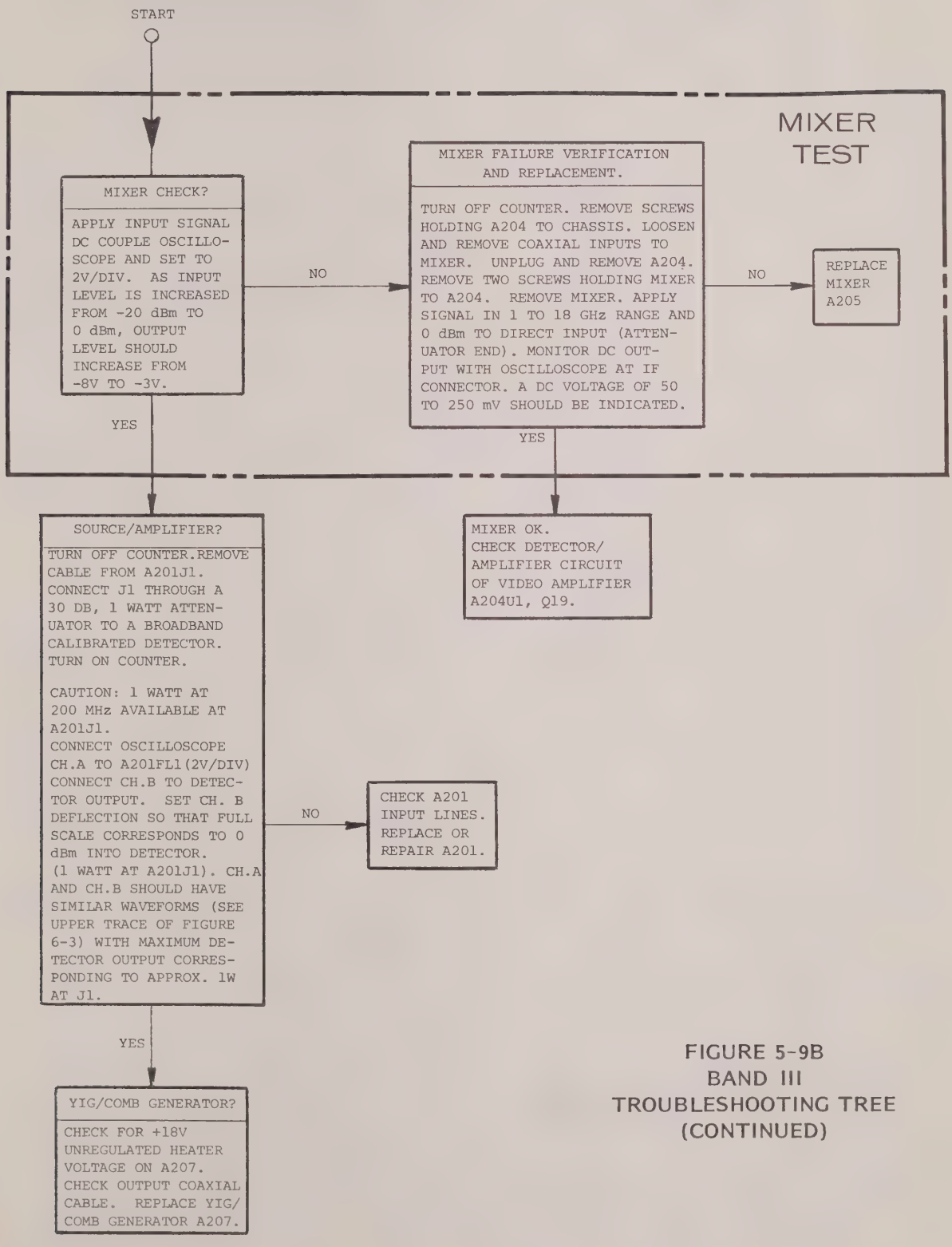

START
MIXER TEST
MIXER CHECK?
APPLY INPUT SIGNAL DC COUPLE OSCILLOSCOPE AND SET TO 2V/DIV. AS INPUT LEVEL IS INCREASED FROM -20 dBm TO 0 dBm, OUTPUT LEVEL SHOULD INCREASE FROM -8V TO -3V.
NO
MIXER FAILURE VERIFICATION AND REPLACEMENT.
TURN OFF COUNTER. REMOVE SCREWS HOLDING A204 TO CHASSIS. LOOSEN AND REMOVE COAXIAL INPUTS TO MIXER. UNPLUG AND REMOVE A204. REMOVE TWO SCREWS HOLDING MIXER TO A204. REMOVE MIXER. APPLY SIGNAL IN 1 TO 18 GHz RANGE AND 0 dBm TO DIRECT INPUT (ATTENUATOR END). MONITOR DC OUTPUT WITH OSCILLOSCOPE AT IF CONNECTOR. A DC VOLTAGE OF 50 TO 250 mV SHOULD BE INDICATED.
NO
REPLACE MIXER A205
YES
YES
SOURCE/AMPLIFIER?
TURN OFF COUNTER.REMOVE CABLE FROM A201J1. CONNECT J1 THROUGH A 30 DB, 1 WATT ATTENUATOR TO A BROADBAND CALIBRATED DETECTOR. TURN ON COUNTER.
CAUTION: 1 WATT AT 200 MHz AVAILABLE AT A201J1.
CONNECT OSCILLOSCOPE CH.A TO A201FL1(2V/DIV) CONNECT CH.B TO DETECTOR OUTPUT. SET CH. B DEFLECTION SO THAT FULL SCALE CORRESPONDS TO 0 dBm INTO DETECTOR. (1 WATT AT A201J1). CH.A AND CH.B SHOULD HAVE SIMILAR WAVEFORMS (SEE UPPER TRACE OF FIGURE 6-3) WITH MAXIMUM DETECTOR OUTPUT CORRESPONDING TO APPROX. 1W AT J1.
NO
CHECK A201 INPUT LINES. REPLACE OR REPAIR A201.
MIXER OK. CHECK DETECTOR/ AMPLIFIER CIRCUIT OF VIDEO AMPLIFIER A204U1, Q19.
YES
YIG/COMB GENERATOR?
CHECK FOR +18V UNREGULATED HEATER VOLTAGE ON A207. CHECK OUTPUT COAXIAL CABLE. REPLACE YIG/COMB GENERATOR A207.

FIGURE 5-9B
BAND III
TROUBLESHOOTING TREE
(CONTINUED)

SECTION 6

ADJUSTMENTS & CALIBRATION

6-1. GENERAL

6-2. This section describes the procedures to be followed in order to correctly adjust the 350D/351D Autohet Counter. In general, adjustments should be made only if the instrument is not operating within specifications, or following replacement of components. Test equipment required is specified in Table 5-1. If adjustments do not result in specified performance, refer to Section 5.

IMPORTANT

Many adjustments are dependent upon previous ones. It is essential that care be taken to perform adjustments in exactly the order presented below. Adjustment locations are shown in Figure 6-1.

6-3. POWER SUPPLY ADJUSTMENT

6-4. Prior to any power supply adjustments, the instrument should be allowed to warm-up for at least 20 minutes. All voltages are measured on Counter Interconnect Board A113. Adjustments are made according to the following procedure:

a. Connect DVM to GND on A113.

b. Measure +12 V output. Adjust A107R7 until output is +12.000 ± .010 V.

c. Measure +5 V output. Adjust A107R15 until output is +5.000 ± .010 V.

d. Measure -12 V output. Adjust A107R21 until output is -12.000 ± .010 V.

e. Measure -5.2 V output. Adjust A107R31 until output is -5.200 ± .010 V.

6-5. BAND I ADJUSTMENTS (20 Hz to 300 MHz)

a. High Frequency Board (A106) Sensitivity:

(1) Set BAND SELECT switch to Band I. Set Mode switch to 10 MHz - 300 MHz.

(2) Connect a 300 MHz CW signal at -10 dBm to the Band I input connector.

(3) Adjust A106R12 until a correct frequency reading is obtained.

(4) Reduce output of signal generator until counter gives an incorrect reading.

(5) Repeat steps (3) and (4) until output of signal generator is at the lowest level which will give a correct reading.

b. Preamplifier (A111) Sensitivity:

(1) Set Band I Mode switch to the 20 Hz - 135 MHz position.

(2) Connect a 50 ohm terminated 135 MHz CW signal at -10 dBm to the Band I input connector.

(3) Adjust A111R17 until a correct frequency reading is obtained.

(4) Reduce output of signal generator until counter gives an incorrect reading.

(5) Repeat steps (3) and (4) until the output of the signal generator is at the lowest level which will give a correct reading.

6-6. BAND II ADJUSTMENTS (100 MHz to 850 MHz)

a. Threshold:

(1) Set BAND SELECT switch to Band II.

(2) Connect a 100 MHz CW signal at -20 dBm to the Band II input connector.

(3) Adjust A109R41 until the reading just drops to all zeros.

6-7. BAND III ADJUSTMENTS (825 MHz to 12.4/18 GHz)

a. Peak Detector offset null:

(1) Set BAND SELECT switch to Band III.

(2) Place A203 on Extender Card (EIP Part Number 5260021).

(3) Ground A203U5 pin 3. CAUTION: Shorting case to ground will result in permanent damage to U5.

(4) Connect DVM to A203U5 pin 6.

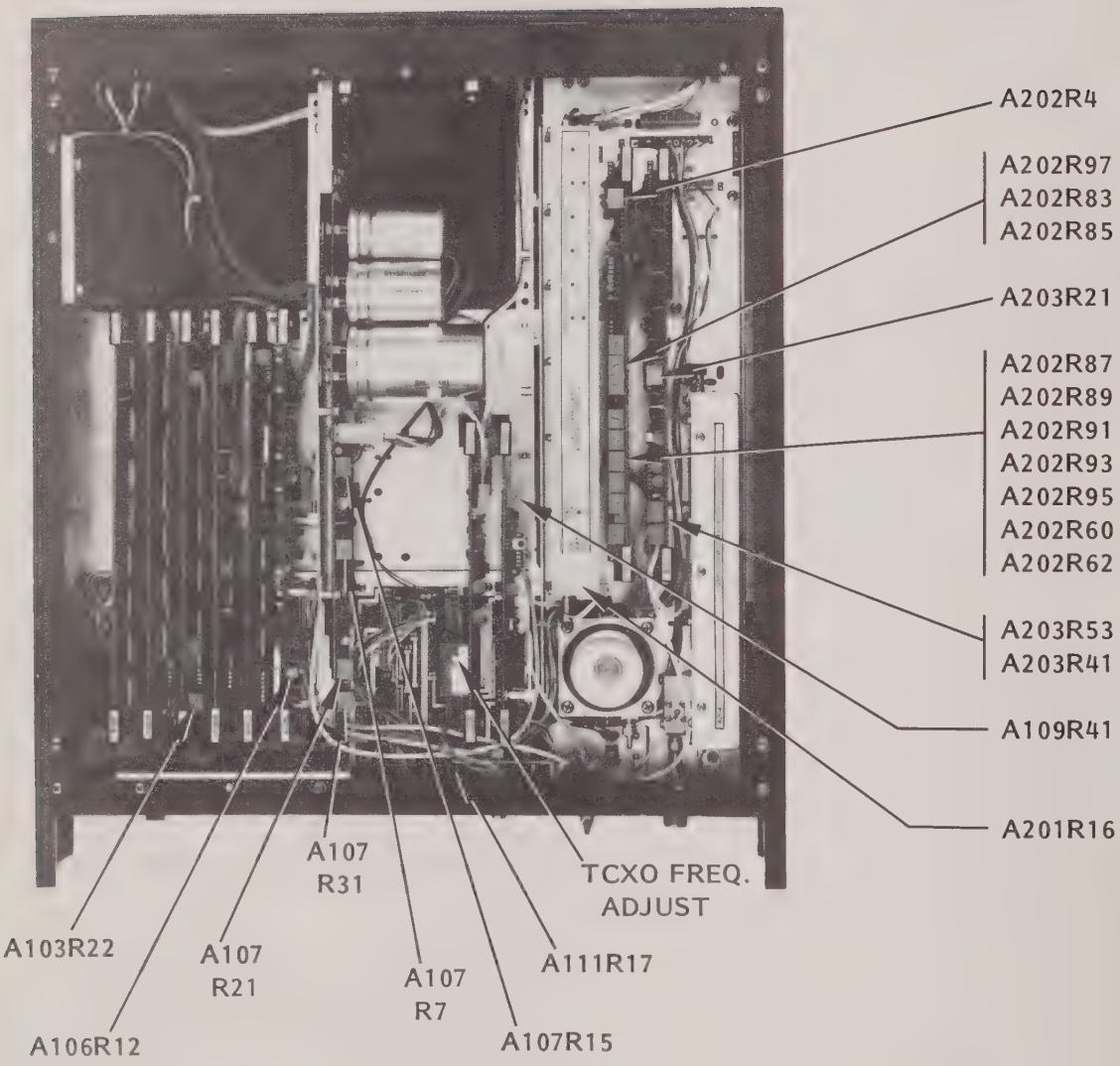


FIGURE 6-1
CALIBRATION
ADJUSTMENT
LOCATOR

(5) Adjust A203R53 for 0.000 ± 1 millivolt.

(6) Remove ground from A203U5 pin 3.

b. Video Detector Gain (see also Paragraph 6-7g.):

(1) Disconnect cable from output of Video Amplifier (A204).

(2) Connect a 150 MHz CW signal at -6 dBm to Cable A203P2 (W21).

(3) Connect DVM to Converter Control 1 Test Point A203TP7.

(4) Adjust A203R41 for 340 ± 20 millivolts.

(5) Reconnect cable W21 to A204 output.

c. In-Band Detector switching point:

(1) Connect sweep generator to A203P2. Set controls as follows:

Sweep	265 MHz downward to 235 MHz
Level	0 dBm
Markers	Every 10 MHz

(2) Connect dual trace oscilloscope as follows:

Horizontal	To sweep generator
Ch. A	A203TP5 via vertical output on sweep generator.

(3) Adjust A203R21 so the switching spike is coincident with the 250 MHz marker as shown in Figure 6-2.

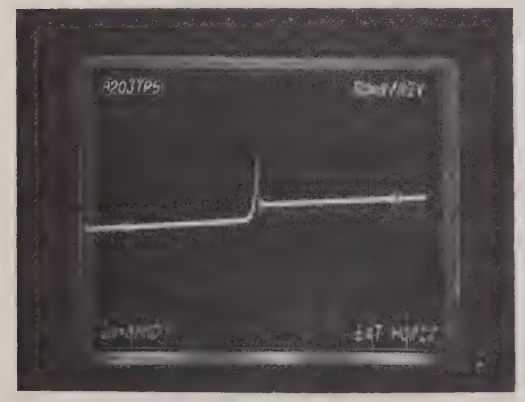


FIGURE 6-2
IN-BAND DETECTOR SWITCHING POINT

d. Preliminary Comb Leveling/Bias:

(1) Set Bias Adjust (A201R16) fully counterclockwise.

(2) Connect dual trace oscilloscope as follows:

Ch. A	A204J3 (Mixer detected output)
Ch. B	A201FL1 (Power Level input)
Ext. Trig.	A203U10 pin 11 (CONV. RESET)

(3) Set Channel A for AC coupling, 100 mV/cm. Set Channel B for DC coupling, 2 V/cm.

(4) Terminate Band III input connector in 50 ohms (a 6 dB or greater attenuation is adequate).

(5) Adjust potentiometers on A202 so the maximum comb line amplitude does not appreciably exceed the levels shown in Table 6-1.

(6) If necessary, readjust A201R16 slightly for optimum flatness. A typical oscilloscope display is shown in Figure 6-3.

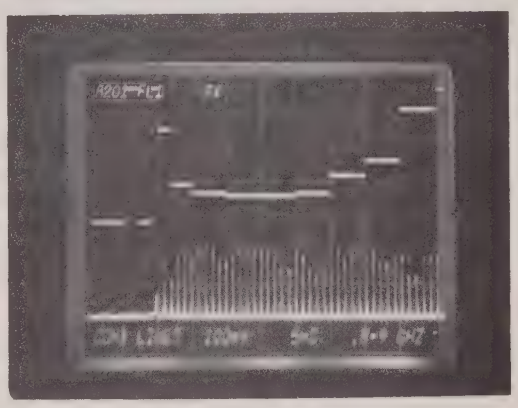


FIGURE 6-3
COMB LEVEL ADJUSTMENTS

e. YIG Driver Offset and Slope:

For this adjustment a Summing Amplifier capable of providing a variable DC offset is recommended. This may be constructed as shown in the schematic of Figure 5-1. Alternatively, a dual trace oscilloscope with differential inputs (such as HP1200A) may be used by applying the signal to one side of the differential input and a variable power supply to the other.

(1) Connect dual trace oscilloscope as follows:

Ch. A	A203TP7 (Video Detector Output)
Ch. B	A202J3 pin 1 (Ramp) via Summing Amplifier
Ext. Trig.	A203U10 pin 11 (CONV. RESET)

(2) Ground A203TP2.

(3) Apply a signal of approximately 1.1 GHz at -15 dBm to Band III input.

(4) Depress RESET switch.

(5) With no DC offset applied, adjust Channel B vertical sensitivity so each ramp step is two vertical divisions (approximately 10 mV/div). Set Channel A to 200 mV/div. Set time base to 5 ms/cm and set time base multiplier to X10. Oscilloscope display should appear as shown in Figure 6-4.

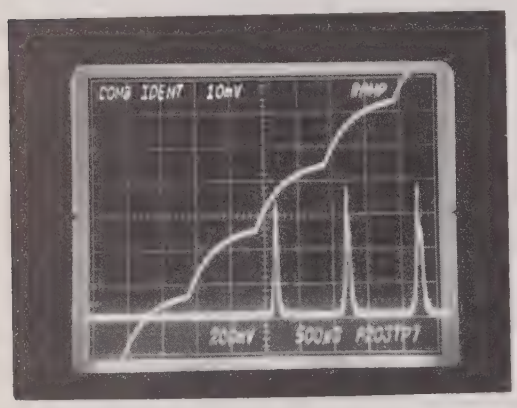


FIGURE 6-4
1 GHz COMB LINE IDENTIFICATION

(6) Reduce the input frequency to 1.0 GHz. When the input frequency is exactly 1 GHz, the center line of the three comb lines on Channel A should null. This identifies the 1 GHz comb line. The 800 MHz comb line is the line preceeding the 1 GHz line.

(7) Remove the ground from A203TP2 and place it on A203TP4. Depress the RESET switch.

(8) Adjust YIG Offset A202R62 so the ramp resets at 40% (.8 div) of the fourth ramp step (50% on 350D). (See Figure 6-5.)

(9) Tune slowly from 1 GHz to 18 GHz. As the frequency is changed, adjust the DC offset and the horizontal position control of the oscilloscope to maintain the upper portion of the ramp on the display. Above 10 GHz, the time base will need to be increased to 10 msec/div.

As the frequency is changed, adjust YIG Slope A202R60 so the ramp reset occurs in the range of 40% to 60% of the full step amplitude at 18 GHz. Adjust R60 so reset occurs at 60% of the step amplitude (50% at 12.4 GHz on the 350D).

(10) Recheck YIG Offset A202R62 and readjust at 1 GHz if necessary. If A202R62 is readjusted, it will be necessary to reset YIG Slope A202R60 at 18 GHz.

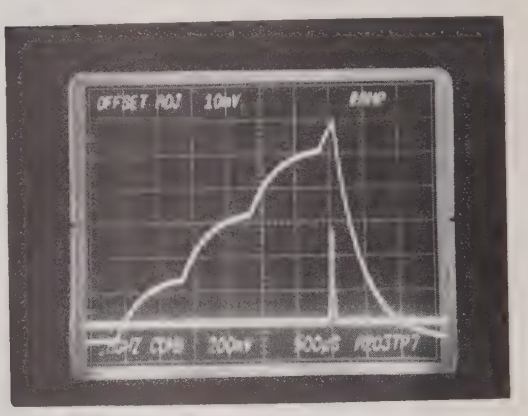


FIGURE 6-5
YIG DRIVER OFFSET ADJUSTMENT

f. YIG Delay Correction

(1) With connections as in paragraph 6.7e, set input frequency to 1 GHz at -15 dBm, and oscilloscope time base control to 10 ms/div., unexpanded.

(2) Adjust YIG Delay Correction A202R4 so display appears approximately as shown in Figure 6-6.

(3) Set time base to variable (approx. 5 ms/div) and externally trigger oscilloscope from A203P1 pin 12 (DAC 2 ENABLE). Adjust oscilloscope time base so DAC 2 ramp occupies the full screen.

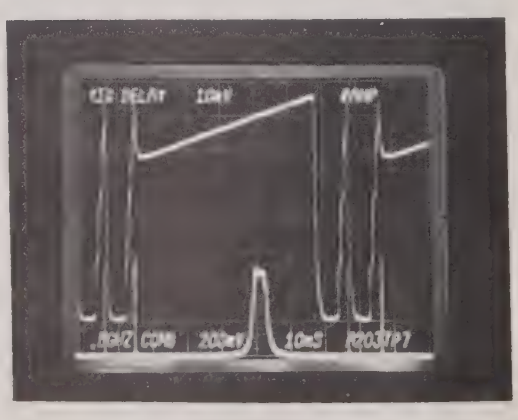


FIGURE 6-6
YIG DELAY CORRECTION 1

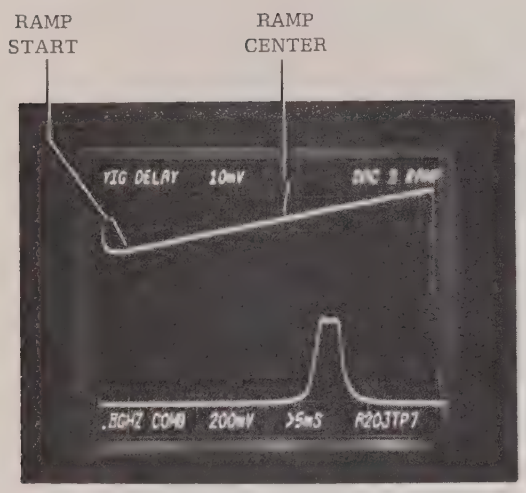


FIGURE 6-7
YIG DELAY CORRECTION 2

(4) Adjust A202R4 so the 50% point of the leading edge of the video pulse occurs one division to the right of center of the DAC 2 ramp as shown in Figure 6-7. Note that the point marked "Ramp Start" is 3 msec after DAC 2 ENABLE, and that the point marked "Ramp Center" is not the center of of the display.

(5) Tune to 18 GHz (12.4 on 350D) and observe position of leading edge with respect to DAC 2 "Ramp Center". This should be approximately one division to the left of "Ramp Center".

(6) If necessary readjust A202R4 until the leading edge of the video pulse is the same distance to the right of "Ramp Center" at 1 GHz, as it is to the left of "Ramp Center" at 18 GHz.

g. Optional Video Detector Gain Adjustment

The procedure given in paragraph 6-7b is approximate and will not necessarily result in the best possible instrument sensitivity. Since this adjustment determines the minimum level from the Video Amplifier to which the Converter will lock, proper adjustment is important where optimum sensitivity is required. The following optional procedure will result in optimum sensitivity. Regardless of whether this step is performed, paragraph 6-7b should be performed in its proper sequence.

A stable source within the Band III frequency range and with variable output power is required. Short term stability should be 1 kHz or better.

(1) Set source power level to -20 dBm.

(2) Observe frequency indication.

(3) Reduce input power slowly while frequently pressing the RESET switch. At some power level counter will fail to lock.

(4) Increase power slightly so that counter just achieves LOCK and a frequency is displayed.

(5) Displayed frequency should be correct (no reduction in indicated frequency). Increase Video Detector gain (adjust A203R41 clockwise) and repeat steps (3) and (4) until an erroneous count is obtained.

(6) Once an erroneous count is obtained, begin decreasing Video Detector gain and repeat steps (3) and (4) until frequency indication is either correct or zero (no LOCK) as power level is varied and counter is reset.

h. Final Comb Leveling/Bias:

The most important function of Comb Leveling is to insure that spurious mixing products (due to doubling of the comb frequency within the Mixer), do not cause erroneous readings. Thus the final leveling procedure insures that maximum output due to these mixing products are below the lock threshold.

(1) Connect Oscilloscope as follows:

Ch. A	A203TP7 (Video Detector output)
Ch. B	A201FL1 (Power Level Control)
Ext. Trig.	A202P1 pin 12 (CONV. RESET)
Time Base	2 ms/div

(2) Ground A203TP2.

(3) Apply a 1.5 GHz signal at -5 dBm and observe the Video Detector signal.

(4) Slowly tune the frequency upward. At some frequencies a spurious output corresponding to about one half the input frequency will be visible. Vary input power to determine the maximum spurious amplitude.

(5) As frequency is varied from 1.5 to 18 GHz, and power is varied to locate the maximum spurious levels, adjust the appropriate controls listed in Table 6-1 so no spurious signal has an amplitude in excess of 200 mV. Refer to Figure 6-8 for a typical display. Vary Time Base setting as necessary to keep display on screen.

ADJUST-MENT	COMB LINE AFFECTED (GHz)	NOMINAL MAXIMUM LEVEL 350D	351D
A202R95	1.0, 1.2	200 mV	200 mV
A202R97	1.4, 1.6, 1.8	200 mV	200 mV
A202R93	2.0, 2.2, 2.4, 2.6, 2.8	200 mV	200 mV
A202R91	3.0, 3.2, 3.4, 3.6, 3.8	200 mV	200 mV
A202R89	4.0, 4.2, 4.4, 4.6, 4.8	200 mV	200 mV
A202R87	5.0, 5.2, 5.4, 5.6, 5.8	200 mV	200 mv
A202R85	6.0, 6.2, 6.4, 6.6, 6.8	300 mV‡	300 mV
A202R83	7.0, 7.2, 7.4, 7.6, 7.8	No Max	300 mV
A202R82*	8.0, 8.2, 8.4, 8.6, 8.8	No Max	300 mV
A202R80*	9.0, 9.2, 9.4, 9.6, 9.8	No Max	300 mv¤

* Selected at Test ‡ 6.0 and 6.2 only ¤ 9.0 GHz only

TABLE 6-1
COMB LEVEL ADJUSTMENTS

CAUTION: Do not attenuate comb lines more than absolutely necessary to maintain maximum spurious outputs of 200 mV. Comb line power relates directly to sensitivity.

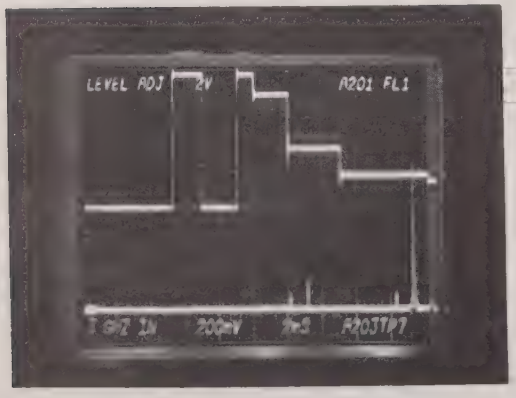


FIGURE 6-8
COMB FREQUENCY HARMONIC GENERATION

6-8. TIME BASE CALIBRATION

IMPORTANT

The precision of time base calibration directly affects overall counter accuracy. Reasons for recalibration, and procedures to be used, should be thoroughly understood before attempting any readjustment.

6-9. The fractional frequency error in the frequency indicated by the counter, is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = -\frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus the inaccuracy associated with a frequency measurement, is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

6-10. TCXO CALIBRATION

6-11. The standard time base oscillator used in the counter is a temperature-compensated crystal oscillator: a TCXO (A116). The highest and lowest actual measured frequencies of this oscillator will differ by no more than 2 parts in 10^6 if the temperature is varied slowly from 0° to +50°C. Therefore, an indicated measurement will exhibit the same fluctuation even though the signal being measured is not changing. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side, the frequency to which it must be set at +25°C. The calibration procedure for this adjustment is described in Paragraphs 6-15 through 6-17.

6-12. At approximate room temperature (+25°C.), the slope of the frequency vs. temperature curve, is normally no worse than -1×10^{-7} parts per °C. Therefore, if the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10 000 000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5°C. will result in a measured signal error due to oscillator temperature characteristics of no more than $\pm 2.5 \times 10^{-7}$ parts. Refer to Paragraphs 6-23 through 6-26 for a recommended adjustment procedure.

6-13. Another source of inaccuracy in the measured signal due to the Time Base Oscillator originates in the natural aging characteristic of the crystal. Aging refers to the long term, irreversible change in frequency, generally in the positive direction, which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is specified to be less than 3×10^{-7} parts per month. This may be expected to improve in time to be no worse than 1×10^{-6} parts per year in continuous service.

6-14. Error due to aging adds directly to error due to temperature perturbations. Thus the frequency of recalibration is dependent upon the overall accuracy requirement of the counter and its environment. For example: If the counter is subjected to the full operating temperature range, and initially adjusted properly, then one month later, the inaccuracy over temperature could be expected to vary from $+ 1.3 \times 10^{-6}$ parts, to $- 0.7 \times 10^{-6}$ parts.

6-15. TCXO CALIBRATION PROCEDURE

NOTICE

For both TCXO recalibration methods: Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

6-16. METHOD 1:

a. Measure the frequency of the TCXO at the rear panel 10 MHz IN/OUT connector, with a second counter of known calibration accuracy.

b. Adjust the TCXO if necessary, by turning the calibration screw on the TCXO case until the measured frequency is the same as that shown on the TCXO calibration label.

6-17. METHOD 2:

a. Apply a 10 000 000 Hz signal from a frequency standard or other oscillator of suitable accuracy and stability to the Band I input of the counter. All RESOLUTION switches should be set to display all the digits including the 1 Hz digit.

b. Adjust the TCXO until the indicated reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example: If the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the displayed reading shows 9 999 997 Hz.

6-18. OVEN STABILIZED OSCILLATOR CALIBRATION

6-19. If one of the Oven Stabilized Oscillator options is installed in the counter (see Section O), the effects of temperature perturbations and aging must still be considered, although the magnitude of these inaccuracies associated with each oscillator are greatly reduced.

6-20. Full benefit of the Oven Stabilized Oscillator characteristics can only be realized if the Oscillator is running continuously: that is, with the counter always connected to a source of AC power. Under these conditions, the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from +25°C. The aging characteristic is also generally in the positive direction.

6-21. The frequency of readjustment of the Oven Stabilized Oscillator is determined by the level of accuracy required. A method of adjusting the oscillator to an inaccuracy of less than 1×10^{-9} parts, relative to a standard, is given in Paragraphs 6-22 through 6-26.

6-22. OVEN STABILIZED OSCILLATOR TEST PROCEDURE

NOTE: This procedure is also usable with the TCXO under the conditions described in Paragraph 6-12.

6-23. TEST EQUIPMENT REQUIRED:

See Table 5-1.

6-24. Figure 6-9 shows the test set-up for determining the frequency of the Oven Stabilized Oscillator (A112). The frequency inaccuracy, relative to a standard, is determined by observing the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\Delta f}{f}$$

For example: If the pattern drifts at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.

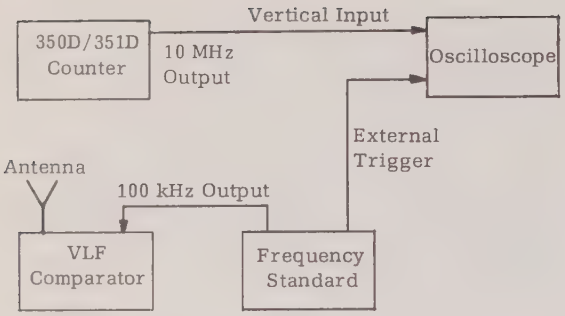


FIGURE 6-9
TIME BASE CALIBRATION

6-25. All frequency checks and adjustments should be made only after the Oven Stabilized Oscillator has been connected to its operating power supply for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours, it may require 72 hours of continuous operation to achieve the specified frequency aging rate (refer to paragraph 7-12).

6-26. TO MEASURE OSCILLATOR FREQUENCY:

a. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.

b. Trigger oscilloscope externally with the frequency standard. The VLF Comparator is used to determine the absolute frequency of the standard.

c. Set oscilloscope sweep rate to 0.1 μ sec/cm and expand X10; this results in a sweep rate of .01 μ sec/cm.

d. Adjust oscilloscope vertical controls for maximum gain.

e. Determine the frequency difference (see para. 6-24).

f. Horizontal drift of oscilloscope display in μ sec/sec, is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting. NOTE: For highest accuracy, the counter should be operated for 72 hours prior to adjustment.

6-27. DISPLAY ADJUSTMENT

a. Numerical display brightness can be adjusted as desired with A103R22. Turn control clockwise to increase brightness.

6-28. Instrument calibration is now complete.

SECTION 7

PERFORMANCE TESTS

7-1. GENERAL

7-2. The purpose of this section is to enable the user to verify that the counter meets specifications over the entire frequency range.

7-3. VARIABLE LINE VOLTAGE

7-4. During the performance tests the 350D/351C should be connected to the power source through a variable voltage device so that line voltage may be varied ± 10% from nominal (115 or 230 Vac) to assure proper operation of the counter under various supply conditions.

7-5. RECOMMENDED TEST EQUIPMENT

7-6. See Table 5-1 for recommended test equipment. Other equipment may be used provided that performance is equal to, or better than, that listed in the table.

7-7. PERFORMANCE TESTS

7-8. RANGE AND SENSITIVITY — BAND I (20 Hz to 135 MHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT switch: Fully left to Band I position.

(3) Mode switch: Set to 20 Hz - 135 MHz position.

(4) TIME BASE switch: Set to INT.

b. Connect signal source output to Band I input via 50 ohm shunt feedthru resistor (to terminate source).

c. Set signal level to 25 mV rms (-19 dBm into 50 ohms).

d. Vary signal from 20 Hz to 135 MHz (changing signal source as required). Counter should display correct input frequency.

7-9. RANGE AND SENSITIVITY — BAND I (10 MHz to 300 MHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT switch: Fully left to Band I position.

(3) Mode switch: Set to 10 MHz - 300 MHz position.

(4) TIME BASE switch: Set to INT.

b. Connect signal source output to Band I input.

c. Vary signal frequency from 10 MHz to 300 MHz at -20 dBm (22 mV rms) power level. Counter should display correct input frequency.

7-10. RANGE AND SENSITIVITY — BAND II (100 MHz to 850 MHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT switch: Centered at Band II position.

(3) TIME BASE switch: Set to INT.

b. Connect signal source output to Band II input.

c. Vary signal frequency from 100 MHz to 150 MHz at -15 dBm (40 mV rms) power level. Counter should display correct input frequency.

d. Change level to -20 dBm (22 mV rms). Vary frequency from 150 MHz to 850 MHz. Counter should display correct frequency.

7-11. RANGE AND SENSITIVITY — BAND III (825 MHz to 12.4/18 GHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT: Fully right to Band III position.

(3) TIME BASE switch: Set to INT.

b. Connect leveled source output to Band III input.

c. Vary signal frequency from 825 MHz to 12.4/18 GHz at the following levels:

825 MHz - 1.1 GHz -20 dBm (22 mV rms)
1.1 GHz - 12.4 GHz -25 dBm (12 mV rms)
12.4 GHz - 18.0 GHz -20 dBm (22 mV rms)

Counter should display correct input frequency.

7-12. TIME BASE AGING RATE

(For Options 03, 04, and 05 only)

a. Place counter in constant temperature environment.

b. Allow counter to warm up for 72 hours if the unit has been disconnected from AC power.

c. Connect 10 MHz rear panel output to input of VLF comparator. (If VLF comparator is not equipped to accept 10 MHz inputs, a divider must be provided.)

d. Determine average frequency over a six-hour interval.

> NOTE: Time interval selected should be during periods of maximum stability of received VLF signal. Avoid periods near sunrise or sunset.

e. Determine average frequency over the same six-hour interval 24 hours later. Counter should remain plugged into the power line during this period to keep time base oven temperature constant.

f. The daily aging rate is the difference between the two readings. This should be within the specifications noted for the particular ovenized oscillator (Option 03, 04, or 05).

SECTION 8

PARTS LISTS

8-1. GENERAL

8-2. This section contains information helpful in ordering replacement parts for this counter. Four tables provide sufficient information for identifying a part and obtaining a replacement, either from EIP or from the manufacturer.

8-3. LIST OF TABLES

a. Table 8-1, REFERENCE DESIGNATORS/ABBREVIATIONS: Lists abbreviations used as schematic reference designators, and in parts list descriptions. Note that some components have two distinct "codes" identifying that part. For example: an integrated circuit is identified on schematics as "U"; but in the parts lists as "IC".

b. Table 8-2, LIST OF MANUFACTURERS: Provides a listing of manufacturers names and addresses, and their Federal Supply Code for Manufacturers (FSCM) number. The FSCM number (or an equivalent) is used in the parts lists as the guide to the manufacturer (or supplier) of the part.

c. Table 8-3, MASTER PARTS LIST: This list has an entry for each separate replaceable part used in the counter. Entries are arranged by EIP Part Number and contain a part description plus the manufacturer's part and FSCM number. This table is used with Table 8-4 to completely identify a component part.

d. Table 8-4, REPLACEABLE PARTS LIST: This table provides a detailed component parts listing for all PC Boards and Assemblies where the parts or components are field replaceable. NOTE: Certain assemblies cannot be field repaired, but must be returned to EIP for service. This table is arranged first by Assembly number (A101-, A102, etc.), then by the schematic reference designator (if any) associated with the assembly. The EIP Part Number and condensed description provide the reference to Table 8-3.

8-4. TO ORDER REPLACEMENT PARTS:

a. Send order directly to EIP at the address shown on the title page of this manual.

b. Specify the EIP Part Number, Reference Designation (if any), and a brief description of the part.

c. For parts not listed in the Parts List, specify the function, location, and description of the part required, and the complete model and serial number of the counter.

TABLE 8-1
REFERENCE DESIGNATORS AND ABBREVIATIONS

REFERENCE DESIGNATORS

A	Assembly
B	Battery
C	Capacitor
CR	Diode
DS	Indicator (display)
F	Fuse
J	Jack (receptacle)
K	Relay
L	Inductor
P	Plug or PCB contacts
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
U	Integrated Circuit
W	Wire (cable)
X	Socket or Holder
Q1-3	Q1 through Q3
Q1/2	Q1 and Q2 (matched pair)

ABBREVIATIONS

CER	Ceramic
CNTR	Counter
CNV	Converter
COMP	Composition
CONN	Connector
DI	Diode
ELEC	Electrolytic
FDTH	Feedthrough
FLTR	Filter
FML	Female
GP	General Purpose
IC	Integrated Circuit
INCN	Interconnection PCB
IND	Inductor
K	Kilo (x 1,000)
LED	Light-emitting diode
M	Meg (x 1,000,000)
MF	Metal Film
ML	Male
MP	Mechanical Part
MTCH PR	Matched Pair
PC	Printed Circuit
PCB	PC Board Assembly
PF	Picofarad
PREC	Precision
RSTR	Resistor
S.A.T.	Value or type selected during factory test. Part may not be used.
SW	Switch
TANT	Tantalum
TRIM	Trimmer
UF	Microfarad
UH	Microhenry
VAR	Variable
WW	Wirewound
XFMR	Transformer
XSTR	Transistor

FSCM	MFR NAME,ADDRESS,ZIPCODE
01295	TEXAS INSTRUMENTS INC.,DALLAS,TX 75222
02660	AMPHENOL CONNECTOR DIV.,BUNKER RAMO CORP.,BROADVIEW,IL 60153
02735	SOLID STATE DIV.,RCA CORP.,SOMERVILLE,NJ 08876
04618	AMERICAN PAMCOR INC.,PAOLI,PA 19301
04713	SEMICONDUCTOR DIV.,MOTOROLA INC.,PHOENIX,AZ 85008
05591	GENERAL RESISTANCE DIV.,CHRONETICS INC.,MT.VERNON,NY 10550
06665	PRECISION MONOLITHICS,SANTA CLARA,CA 95050
07263	FAIRCHILD SEMICONDUCTOR, MOUNTAIN VIEW,CA 94040
09353	C AND K COMPONENTS INC.,WATERTOWN,MA 02172
11236	CTS OF BERNE INC.,BERNE,IN 46711
11532	TELEDYNE RELAYS,HAWTHORNE,CA 90250
12436	GENERAL DYNAMICS CORP.,SAN DIEGO,CA 92112
14099	SEMTECH CORP.,NEWBURY PARK,CA 91320
14158	AVX CERAMICS CORP.,SAN DIEGO,CA 92121
14298	AMERICAN COMPONENTS INC.,CONSHOHOCKEN,PA 19428
14433	ITT SEMICONDUCTOR DIV.OF ITT CORP.,W.PALM BEACH,FL 33401
14752	ELECTRO CUBE INC.,SAN GABRIEL,CA 91776
20754	KMC SEMICONDUCTOR CORP.,LONG VALLEY,NJ 07853
21793	DANA LABORATORIES INC.,IRVINE,CA 92664
23880	STANFORD APPLIED ENGINEERING INC.,SANTA CLARA,CA 95050
23936	PAMOTOR INC.,BURLINGAME,CA 94010
24546	CORNING GLASS WORKS,BRADFORD,PA 16701
26654	VARADYNE INC.,SANTA MONICA,CA 90403
27014	NATIONAL SEMICONDUCTOR CORP.,SANTA CLARA,CA 95051
28480	HEWLETT-PACKARD CO.,PALO ALTO,CA 94304
32293	INTERSIL INC.,CUPERTINO,CA 95014
50088	MOSTEK CORP.,CARROLLTON,TX 75006
50522	ELECTRONIC SPECIAL PRODUCTS,MONSANTO CO.,CUPERTINO,CA 95014
56289	SPRAGUE ELECTRIC CO.,NORTH ADAMS,MA 01247
70903	BELDEN CORP.,CHICAGO,IL 60644
71279	CAMBRIDGE THERMIONIC CORP.,CAMBRIDGE,MA 02138
71400	BUSSMAN MFG DIV.,MCGRAW-EDISON CO.,ST.LOUIS,MO 63107
71785	CINCH DIV.,TRW ELECTRONIC COMPONENTS,ELK GROVE VILLAGE,IL 60007
72136	ELECTRO-MOTIVE MFG. CO.,WILLIMANTIC,CT 06226
72259	NYTRONICS INC.,PELHAM MANOR,NY 10803
72982	ERIE TECHNOLOGICAL PRODUCTS INC.,ERIE,PA 16512
73138	HELIPOT DIV.,BECKMAN INSTRUMENTS,FULLERTON,CA 92634
73445	AMPEREX ELECTRONIC CORP.,HICKSVILLE,NY 11802
75915	LITTELFUSE INC.,DES PLAINES,IL 60016
76854	OAK MFG DIV.,OAK ELECTRO/NETICS CORP.,CRYSTAL LAKE,IL 60014
80294	INSTRUMENT DIV.,BOURNS INC.,RIVERSIDE,CA 92506
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT INC.,CHICAGO,IL 60630
86797	ROGAN BROS.INC.,SKOKIE,IL 60076
91637	DALE ELECTRONICS INC.,COLUMBUS,NE 68601
91836	KINGS ELECTRONICS CO.,TUCKAHOE,NY 10707
95275	VITRAMON INC.,BRIDGEPORT,CT 06601
96341	MICROWAVE ASSOCIATES,BURLINGTON,MA 01801
96291	SEALECTRO,MAMARONECK,NY 10544
99392	STM CORP.,OAKLAND,CA 94601
99800	DELAVAN DIV.,AMERICAN PRECISION INDUST.,EAST AURORA,NY 14052
	FOLLOWING MFRS DO NOT HAVE FSCM NUMBER
0000A	MOLEX INC.,LISLE,IL 60532
0000B	STETTNER-TRUSH,CAZENOVIA,NY 13035
0000C	PLESSEY ELECTRO-PRODUCTS,LOS ANGELES,CA 90066
0000L	R-OHM CORPORATION,IRVINE,CA 92664

TABLE 8-2. LIST OF MANUFACTURERS

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
2100002	CAP:CHIP .001UF 20% 50V	95275	VJ1210A102MF
2100005	CAP:CHIP 150PF 100V	26654	3BN100S151K
2150001	CAP:CER .001UF 20% 1KV	56289	5GA-D10
2150003	CAP:CER .01UF 20% 100V	56289	TG-S10
2150004	CAP:CER .1UF 50V	72982	8121M050651104
2150005	CAP:CER .002UF 20% 1KV	56289	5GA-D20
2150006	CAP:CER .02UF 20% 100V	56289	TG-S20
2150008	CAP:CER .005UF 20% 100V	56289	TG-D50
2160002	CAP:CER 1.0PF NPO 500V	72982	301000C0K0109C
2160004	CAP:CER 10PF NPO 500V	72982	301000C0H0100C
2160005	CAP:CER 12PF NPO 500V	72982	301000C0G0120C
2160006	CAP:CER 15PF NPO 500V	72982	301000C0G0150J
2160007	CAP:CER 18PF NPO 500V	72982	301000C0G0180J
2160008	CAP:CER 2.2PF NPO 500V	72982	301000C0J0229C
2160010	CAP:CER 24PF NPO 500V	72982	301000C0G0240J
2160013	CAP:CER 4.7PF NPO 500V	72982	301000C0H0479C
2160014	CAP:CER 6.8PF NPO 500V	72982	301000C0H0689C
2160015	CAP:CER 8.2PF NPO 500V	72982	301000C0H0829C
2160016	CAP:CER 20PF NPO 500V	72982	301000C0G0220J
2200001	CAP:ELEC 1250UF 50V	99392	39CS50GL1251
2200005	CAP:ELEC 28000UF 15V	99392	91C15RB283
2200009	CAP:ELEC 8000UF 15V	99392	39CS15HP83
2200010	CAP:ELEC 8500UF 25V	99392	91C25HA852
2200012	CAP:ELEC 11000UF 15V	99392	39CS15JP113
2250001	CAP:MICA 10PF 5% 500V	72136	DM15CD100D0
2250002	CAP:MICA 100PF 5% 500V	72136	DM15CD101J0
2250005	CAP:MICA 150PF 5% 500V	72136	DM15CD151J0
2250006	CAP:MICA 180PF 5% 500V	72136	DM15CD181J0
2250007	CAP:MICA 2.0PF25% 500V	72136	DM15CD2R0D0
2250009	CAP:MICA 200PF 5% 500V	72136	DM15CD201J0
2250011	CAP:MICA 220PF 5% 500V	72136	DM15CD221J0
2250012	CAP:MICA 27PF 5% 500V	72136	DM15CD270J0
2250013	CAP:MICA 300PF 5% 500V	72136	DM15CD301J0
2250014	CAP:MICA 33PF 5% 500V	72136	DM15CD330J0
2250017	CAP:MICA 47PF 5% 500V	72136	DM15CD470J0
2250018	CAP:MICA 470PF 5% 500V	72136	DM15CD471J0
2250024	CAP:MICA 30PF 5% 500V	72136	DM15CD300J0
2300003	CAP:TANT .15UF 35V	14433	TAG20-0.15/35-50
2300005	CAP:TANT .47UF 35V	14433	TAG20-0.47/35-50
2300006	CAP:TANT 1.0UF 10% 35V	56289	CS13BF105K
2300008	CAP:TANT 1.0UF 35V	14433	TAG20-1.0/35-50
2300010	CAP:TANT 10UF 16V	14433	TAG20-10/16-50
2300015	CAP:TANT 33UF 10V	14433	TAG20-33/10-50
2300016	CAP:TANT 47UF 10% 20V	56289	CS13BE476K
2300017	CAP:TANT 47UF 6.3V	14433	TAG20-47/6.3-50
2300019	CAP:TANT 6.8UF 10% 35V	56289	CS13BF685K
2300020	CAP:TANT .10UF 35V	14433	TAG20-.10/35-50
2300022	CAP:TANT 22UF 20% 20V	14433	TAG20-22/20-20
2300025	CAP:TANT 47UF 20% 16V	14433	TAG20-47/16-20
2350001	CAP:TRIM 2-8PF 250V	0000B	10S-T-22-2/8
2350002	CAP:TRIM 5.5-18PF 250V	0000B	10S-T-22-5.5/18
2350003	CAP:TRIM 8-25PF 250V	0000B	10S-T-22-8/25
2350004	CAP:FLM .0015UF10% 100V	72136	1MDF-1-152K
2350011	CAP,FDTH:RF FILTER,5KPF	14158	2-VB3-50
2350015	CAP:MET FLM .047UF 100V	14752	230B18473
2350017	CAP,FDTH:RF FILTER,5KPF	04618	859556-1
2350022	CAP:TRIM 5.5-18PF 250V	0000B	10S-T-24-5.5/18
2610010	CONN:JACK,BLKHD,RECPT	98291	51-045-0000
2610017	CONN:PLUG,PC RCPT,STR	98291	52-052-0000
2610018	CONN:JACK,PC RCPT,STR	98291	51-051-0000
2610024	CONN:BNC,BLKHD,TRS FNSH	91836	KC-79-35
2620006	CONN:PC WAFER 6PIN ML	0000A	09-18-5061
2620012	CONN:PC WAFER 9PIN, ML	0000A	09-18-5091
2620014	CONN:PC WAFER 4PIN, ML	0000A	09-60-1041
2620016	CONN:PC WAFER, 6PIN, ML	0000A	09-60-1061
2620027	JACK:PC .080 PIN FML	71279	3398-01-03
2620029	CONN:PC RT AN,3PIN, ML	0000A	09-66-1031
2620030	CONN:PC RT AN,4PIN, ML	0000A	09-66-1041
2620031	CONN:PC RT AN,7PIN, ML	0000A	09-66-1071
2620042	CONN:PC WAFER, 9PIN, ML	0000A	09-60-1091
2620044	CONN:PC WAFER,12PIN, ML	0000A	09-60-1121
2620047	CONN:PC WAFER, 5PIN, ML	0000A	09-60-1051
2630003	SOCKET: 14 PIN,NYLON	0000A	A-4497-14
2630009	SOCKET: 14 PIN IC	71785	14-N-DIP
2640004	CONN 50PIN	02660	57-40500
2640005	RECEPTACLE	82389	EAC-301
2704001	DIODE: RECT	04713	1N4001
2704154	DIODE: GEN PURP	07263	1N4154
2704370	DIODE: 2.4V ZENER	04713	1N4370
2704757	DIODE: 51V ZENER	04713	1N4757
2705230	DIODE: 4.7V ZENER	04713	1N5230
2705231	DIODE: 5.1V ZENER	04713	1N5231
2705234	DIODE: 6.2V ZENER	04713	1N5234
2705236	DIODE: 7.5V ZENER	04713	1N5236
2705237	DIODE: 8.2V ZENER	04713	1N5237
2705239	DIODE: 9.1V ZENER	04713	1N5239
2705711	DIODE:HOT CARRIER	28480	1N5711
2710004	DIODE: HOT CARR	07263	FH1100
2710006	DIODE: HOT CARR	28480	5082-2800
2710008	BRDG RECT	14099	SBR05
2710012	DIODE:VOLT VAR CAP	04713	MV109
2710013	DIODE:LO LKGE-DUAL	32293	DX100
2710014	DIODE,MTCH PR:FH1100	EIP	2710004
2710016	DIODE: HOT CARRIER	28480	5082-2835

TABLE 8-3. MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
2710018	BRDG RECT	04713	MDA980-1
2710019	BRDG RECT	14099	SBMB1
2710022	DIODE: PIN	96341	MA47110
2710023	DIODE: TUNNEL,SWITCHING	20754	A00010C
2710024	DIODE: PIN	96341	MA47123
2710028	BRDG RECT	04713	MDA990-1
2710029	BRIDE RECT	04713	MDA970-1
2720827	DIODE: 6.2V ZENER	04713	1N827A
2720963	DIODE: 12V ZENER	04713	1N963A
2800001	LAMP,INDICATOR: RED	50522	MV5021
2800004	IC:NUMERIC IND. RED	28480	5082-7730
2800008	LAMP,LED: GREEN	50522	MV5253
2800013	LAMP:LED,ORG DIFFUSED	50522	MV5153
3000937	IC:HEX INVERTER	27014	DM937N
3007400	IC:QUAD 2INP NAND GATE	27014	DM7400N
3007401	IC:QUAD 2INP NAND GATE	27014	DM7401N
3007402	IC:QUAD 2INP NOR GATE	27014	DM7402N
3007404	IC:HEX INVERTER	27014	DM7404N
3007405	IC:HEX INVERTER	27014	DM7405N
3007408	IC:QUAD 2INP AND GATE	01295	SN7408N
3007411	IC:TRI 3INP AND GATE	27014	DM7411N
3007427	IC:TRIPLE 3INP NOR GATE	27014	DM7427N
3007432	IC:QUAD 2INP OR GATE	27014	DM7432N
3007442	IC:BCD/DEC DECODER	27014	DM7442N
3007447	IC:BCD/7SEG DECODER	27014	DM7447N
3007454	IC:4WIDE 2INP AOI GATE	27014	DM7454N
3007473	IC:DUAL J-K F/F	27014	DM7473N
3007475	IC:QUAD LATCH	27014	DM7475N
3007476	IC:DUAL J-K F/F	27014	DM7476N
3007490	IC:DECADE COUNTER	27014	DM7490N
3007493	IC:4BIT BINARY COUNTER	27014	DM7493N
3008601	IC:RETRIG ONE SHOT	27014	DM8601N
3010615	IC:UHF CNTR-DIVIDE/4	0000C	SP8615B
3010637	IC:UHF BCD DEC CNTR	0000C	SP8637B
3011039	IC:QUAD TRANSLATOR	04713	MC1039P
3011414	IC:DUAL DIFF COMP	04713	MC1414L
3011670	IC:D-TYPE F/F	04713	MC1670L
3014044	IC:PHASE/FREQ DETECTOR	04713	MC4044P
3035009	IC:P CHAN MOS DIVIDER	50088	MK5009N
3040001	IC:OP AMPL,HI SLEW RATE	06665	OP-01CJ
3040304	IC:VOLT REG	27014	LM304
3040305	IC:VOLT REG	27014	LM305
3040417	IC:BROAD BAND AMPL	73445	ATF417
3040741	IC:OP AMPL	27014	LM741CN
3041741	IC:OP AMPL,HI SLEW RATE	04713	MC1741SCP1
3043049	IC:DUAL/DIFF AMPL	02735	CA3049T
3048007	IC:FET/OP AMPL	32293	8007C
3074123	IC:TTL/MONOSTABLE MV	01295	DM74123N
3074153	IC:DUAL 4/1 MULTIPLEXR	27014	DM74153N
3074155	IC:DUAL 2/4LINE DECODR	27014	DM74155N
3074176	IC:PRESET DEC COUNTER	27014	DM74176N
3074192	IC:DUAL CLOCK W/CLEAR	27014	DM74192N
3074196	IC:PST DECADE COUNTER	01295	SN74196N
3090002	IC:QUAD 2INP AND GATE	27014	DM74H08N
3090003	IC:DUAL 4INP AND GATE	27014	DM74H21N
3110105	IC:TRI OR GATE	04713	MC10105L
3110131	IC:DUAL D F/F	04713	MC10131L
3110138	IC:BI-QUINARY COUNTER	04713	MC10138P
3112000	IC:DIGITAL MIXER/TRANS	04713	MC12000P
3510001	INDUCTOR: 0.1UH	72259	DD-0.10
3510003	INDUCTOR: 1.0UH	72259	DD-1.00
3510004	INDUCTOR: 0.22UH	72259	DD-0.22
3510005	INDUCTOR: 2.2UH	72259	DD-2.20
3510007	INDUCTOR: .33UH	99800	1025-08
3510008	INDUCTOR: 0.15UH	99800	1025-00
3510009	INDUCTOR: 0.68UH	72259	DD-0.68
3510010	INDUCTOR: 1.2UH	99800	1025-22
3510011	INDUCTOR: 0.12UH	72259	DD-0.12
3520007	INDUCTOR: 100 UH	99800	1537-76
3900003	RELAY:SIGNAL,DPDT	11532	712-12
4000XXX	RSTR:COMP,OHMS+-5%,1/8W	81349	RC05GFXXXJ
4000999	RSTR:COMP-SLECT AT TEST	81349	RC05GFXXXJ
4010XXX	RSTR:COMP,OHMS+-5%,1/4W	81349	RC07GFXXXJ
4010999	RSTR:COMP-SLECT AT TEST	81349	RC07GFXXXJ
4020XXX	RSTR:COMP,OHMS+-5%,1/2W	81349	RC20GFXXXJ
4051002	RSTR:PREC 10K OHM 1%	81349	RN55C1002F
4051212	RSTR:PREC 12.1K OHM 1%	81349	RN55C1212F
4051501	RSTR:PREC 1.5K OHM 1%	81349	RN55C1501F
4051622	RSTR:PREC 16.2K OHM 1%	81349	RN55C1622F
4051912	RSTR:PREC 19.1K OHM 1%	81349	RN55C1912F
4052002	RSTR:PREC 20K OHM 1%	81349	RN55C2002F
4052003	RSTR:PREC 200K OHM 1%	81349	RN55C2003F
4053922	RSTR:PREC 39.9K OHM 1%	81349	RN55C3922F
4054992	RSTR:PREC 49.9K OHM 1%	81349	RN55C4992F
4057500	RSTR:PREC 750 OHM 1%	81349	RN55C7500F
4061101	RSTR:PREC 1.1K OHM 1%	81349	RN55D1101F

TABLE 8-3. MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
4061472	RSTR:PREC 14.7K OHM 1%	81349	RN55D1472F
4062152	RSTR:PREC 21.5K OHM 1%	81349	RN55D2152F
4062261	RSTR:PREC 2.26K OHM 1%	81349	RN55D2261F
4062431	RSTR:PREC 2.43K OHM 1%	81349	RN55D2431F
4062871	RSTR:PREC 2.87K OHM 1%	81349	RN55D2871F
4065621	RSTR:PREC 5.62K OHM 1%	81349	RN55D5621F
4065761	RSTR:PREC 5.76K OHM 1%	81349	RN55D5761F
4068661	RSTR:PREC 8.66K OHM 1%	81349	RN55D8661F
4101003	RSTR:PREC 100K OHM .1%	14298	AME55-C3-1003B
4101004	RSTR:PREC 1M OHM 1%	14298	AME57-C1-1004F
4102003	RSTR:PREC 200K OHM.25%	14298	AME55-C3-2003C
4104003	RSTR:PREC 400K OHM .5%	14298	AME55-C1-4003D
4105003	RSTR:PREC 500K OHM .5%	14298	AME55-C1-5003D
4108002	RSTR:PREC 80K OHM .1%	14298	AME55-C3-8002B
4110003	RSTR:WW 5 OHM 1% 7W	12436	T7(10PPM)
4110004	RSTR:WW 0.5 OHM 3% 2W	91637	RS-2B
4110006	RSTR:WW 0.33 OHM 3% 4W	91637	RS-2
4110007	RSTR:WW 0.2 OHM 3% 5W	91637	RS-5
4110012	RSTR:WW 0.66 OHM 3% 4W	91637	RS-2
4110013	RSTR:WW 0.15 OHM 3% 5W	91637	RS-5
4120004	RSTR:CBN FLM 5.6 OHM 5%	0000L	R25-5.6-5%-1/4W
4120008	RSTR:CBN FLM 8.2 OHM 5%	0000L	R25-8.2-5%-1/4W
4130XXX	RSTR:MET OX,100PPM,1/4W	24546	C4/2%/CHMS
4130999	RSTR:MTOX-SLECT AT TEST	24546	C4/2%/XXX
4140029	RSTR:PREC 4K OHM .01%	05591	TYPE 4S8P1S8
4140030	RSTR:PREC 8K OHM .01%	05591	TYPE 4S8P1S8
4140031	RSTR:PREC 10K OHM .01%	05591	TYPE 4S8P1S8
4140032	RSTR:PREC 20K OHM.025%	05591	TYPE 4S8P1S8
4140033	RSTR:PREC 40K OHM .05%	05591	TYPE 4S8P1S8
4140034	RSTR:PREC 3K OHM .1%	05591	TYPE 4S8P1S8
4140035	RSTR:PREC 8K OHM .1%	05591	TYPE 4S8P1S8
4140039	RSTR:PREC 3.7K OHM .1%	05591	TYPE 4S8P1S8
4150XXX	RSTR:MET OX,100PPM,1/8W	24546	C3/2%/CHMS
4150999	RSTR:MTOX-SLECT AT TEST	24546	C3/2%/XXX
4250001	RSTR:VAR CER 100 OHM	73138	72XWR100
4250003	RSTR:VAR CER 1K OHM	73138	72XWR1K
4250005	RSTR:VAR CER 5K OHM	73138	72XWR5K
4250006	RSTR:VAR CER 10K OHM	73138	72XWR10K
4250008	RSTR:VAR CER 100K OHM	73138	72XWR100K
4250009	RSTR:VAR CER 500 OHM	73138	72XWR500
4260001	RSTR:VAR CER 10K OHM	80294	3059J-1-103M
4280009	RSTR:VAR WW 500 OHM	73138	89PR-500
4290001	RSTR:VAR 250K/SPDT SW	11236	EF8078/RVF45
4500007	SWITCH:P/B,8-STATION	EIP	SRCE CONT DWG
4500008	SWITCH:P/B (PWR IND)	EIP	SRCE CONT DWG
4510001	SWITCH:TOG,SPDT,120V,5A	09353	7101H
4520006	SW:SLD,2-DPDT (PWR CHG)	82389	47227LFE
4530008	SWITCH:LEVER (BAND SEL)	76854	555462723-184EA1
4540002	SWITCH,THUMBWHEEL: BCD	23880	900048
4703563	XSTR: NPN	07263	2N3563
4703641	XSTR: NPN SW	07263	2N3641
4704124	XSTR: NPN GP	04713	2N4124
4704126	XSTR: PNP GP	04713	2N4126
4704258	XSTR: PNP RF	07263	2N4258
4704401	XSTR: NPN	04713	2N4401
4704416	XSTR: N-CHAN JFET	04713	2N4416
4704959	XSTR: PNP RF	04713	2N4959
4705983	XSTR: NPN PWR	04713	2N5983
4705989	XSTR: NPN PWR	04713	2N5989
4710002	XSTR: PNP PWR	04713	MJE370
4710003	XSTR: NPN PWR	04713	MJE520
4710005	XSTR: UNIJCT	04713	MU4891
4710007	XSTR: NPN PWR	04713	MJE371
4710009	XSTR: PNP	04713	MJE350
4710010	XSTR: PNP RF	04713	MPS-H81
4710011	XSTR:GRADED 2N5179-RED	EIP	4705179
4710012	XSTR:GRADED 2N5179-YEL	EIP	4705179
4710013	XSTR:GRADED 2N5179-GRN	EIP	4705179
4710014	XSTR:MTCH PR,2N5179-RED	EIP	4710011
4710015	XSTR:MTCH PR,2N5179-YEL	EIP	4710012
4710017	XSTR:NPN RF SW	04713	MMT3960
4710018	XSTR: PNP AMPL	04713	MPS-L51
4710019	XSTR: PNP AMPL	04713	MPS-D55
4720002	XSTR: NPN RF	04713	2N3866(MOT)
4900002	TRANSFORMER,POWER	EIP	SRCE.CONT.DWG.
4900004	TRANSFORMER,POWER	EIP	SPEC.CONT.DWG
5000012	FAN,AXIAL,115VAC	23936	8500
5000052	FUSE HOLDER	75915	348877
5000055	TILT BAIL	21793	453458
5000056	KNOB:RND W/INSERT .51D	86797	RB67-0ML.25SHFT
5000079	FUSE: .750A,SB,3AG,250V	71400	MDL-3/4A
5000101	FUSE: 1.5A,SB,3AG,250V	71400	MDX-1-1/2
5000104	TERMINAL,INSULATED	71279	1502-1-05
5210023	COVER,ENCL: TOP	21793	453453
5210024	COVER,ENCL: BOTTOM	21793	453454
5220002	PAD,RUBBER:ENCL FOOT	EIP	M/F:5660004
5280013-01	CAP:MODIFIED TG-S10	EIP	M/F:2150003
5440002	LINE CORD SET, 3-COND	70903	17250

REF	SAME	EIP P/N	DESCRIPTION
A1 (BASIC COUNTER CHASSIS COMPONENTS)			
A1B1		5000012	FAN
A1F1 (115V)		5000101	FUSE: 1.5A, S/B
A1F1 (230V)		5000079	FUSE: .75A, S/B
A1J1		2640005	AC PWR RECEPT
A1J2		2640004	(OPT 09)
A1J3	J2		(OPT 01, 06, 07)
A1J4		2610024	(10 MHz)
A1J111-112		2610024	(BAND I, II INP)
A1J113		2030003	(ASSY A206)
A1MP1		5000056	KNOB (SMPL RT)
A1MP2		5000055	TILT BAIL
A1MP3		5210023	TOP COVER
A1MP4		5210024	BOTTOM COVER
A1MP5		5220002	MOUNTING FOOT
A1MP6		5440002	POWER CORD
A1S1		4500008	(POWER)
A1S2		4530008	(BAND SELECT)
A1S102		4520006	(115/230)
A1S103		4510001	(INT/EXT)
A1T1		4900004	MAIN PWR XFMR
A1XF1		5000052	FUSE HOLDER

PCB ASSY A101 P/N: 2020036 COUNT CHAIN 1

REF	SAME	EIP P/N	DESCRIPTION
C1		2150003	C: CER .01 UF
C2		2300015	C: TANT 33 UF
C3-4	C1		
C5		2250011	C: MICA 220 PF
C6-10	C1		
C11	C5		
R1-6		4010332	R: COMP 3.3K
R7		4010391	R: COMP 390
R8-11		4010122	R: COMP 1.2K
R12		4010222	R: COMP 2.2K
R13-14	R8		
R15-21		4010101	R: COMP 100
R22	R7		
U1		3007490	IC: DEC CNTR
U2		3007493	IC: 4-BIT CNTR
U3		3007402	IC: NOR GT
U4		3007404	IC: HEX INVERT
U5	U1		
U6	U4		
U7	U3		
U8	U4		
U9	U1		
U10		3007401	IC: QUAD GT
U11		3007411	IC: AND GT
U12	U3		
U13		3007408	IC: QUAD GT
U14	U3		
U15		3074176	IC: DEC CNTR
U16	U4		
U17		3007454	IC: AOI GT
U18		3007400	IC: NAND GT
U19	U3		
U20	U18		
U21		3007405	IC: HEX INVERT
U22		3007447	IC: DECODER
U23-24		3007476	IC: DUAL F/F

PCB ASSY A102 P/N: 2020034 COUNT CHAIN 2

REF	SAME	EIP P/N	DESCRIPTION
C1		2300015	C: TANT 33 UF
C2-4		2150003	C: CER .01 UF
J1-4		2630003	SOCKET: 14 PIN
R1		4010222	R: COMP 2.2K
R2		4010122	R: COMP 1.2K
R3	R1		
R4-17		4010101	R: COMP 100
R18-19	R2		
R20		4010596	R: COMP 5.6
R21-23	R2		
U1-2		3007447	IC: DECODER
U3		3007405	IC: HEX INVERT
U4		3074176	IC: DEC CNTR
U5		3007475	IC: QUAD LATCH
U6		3074153	IC: MPLXR
U7	U4		
U8	U5		
U9	U6		
U10	U4		
U11	U5		
U12	U4		
U13	U5		
U14	U6		
U15	U4		
U16	U5		
U17	U6		
U18	U4		
U19	U5		
U20		3007432	IC: QUAD GT
U21	U5		

PCB ASSY A103 P/N: 2020051 COUNT CHAIN 3

REF	SAME	EIP P/N	DESCRIPTION
C1		2150003	C: CER .01 UF
C2		2159999	C: CER S.A.T.
C3	C1		
C4		2300015	C: TANT 33 UF
C5-6	C1		
C7		2300010	C: TANT 10 UF
C8	C1		
C9	C4		
C10	C1		

TABLE 8-4. REPLACEABLE PARTS LIST

REF	SAME	EIP P/N	DESCRIPTION
CR1-8		2705711	DI: HOT CARR
CR9		2704154	DI: GP
Q1-3		4710012	XSTR: SELECT
Q4		4704124	XSTR: NPN GP
Q5		4704126	XSTR: PNP GP
Q6	Q1		
Q7	Q5		
Q8		4710003	XSTR: NPN PWR
R1		4010131	R: COMP 130
R2		4010361	R: COMP 360
R3		4010200	R: COMP 20
R4		4010271	R: COMP 270
R5		4010121	R: COMP 120
R6		4010431	R: COMP 430
R7		4010391	R: COMP 390
R8		4010102	R: COMP 1K
R9-12		4010222	R: COMP 2.2K
R13	R9		
R14	R8		
R15		4010330	R: COMP 33
R16		4010332	R: COMP 3.3K
R17	R8		
R18		4010471	R: COMP 470
R19	R7		
R20		4250009	R: VAR 500
R21		4010821	R: COMP 820
R22	R8		
U1		3007405	IC: HEX INV
U2		3074196	IC: DEC CNTR
U3-5		3074176	IC: DEC CNTR
U6		3007442	IC: DECODER
U7-10		3007475	IC: QUAD LTCH
U11		3007427	IC: NOR GT
U12		3007454	IC: AOI GT
U13-14		3074153	IC: MPLXR

PCB ASSY A104 P/N: 2020010 CONTROL 2

REF	SAME	EIP P/N	DESCRIPTION
C1		2150003	C: CER .01 UF
C2-3		2300015	C: TANT 33 UF
C4	C1		
C5		2300010	C: TANT 10 UF
C6		2150001	C: CER .001 UF
C7		2300017	C: TANT 47 UF
C8-9	C5		
C10-11	C1		
C12-14	C6		
C15	C1		
C16	C6		
CR1-5		2704154	DI: SIG
Q1-3		4704126	XSTR: PNP GP
Q4		4704124	XSTR: NPN GP
Q5	Q1		
Q6-7	Q4		
Q8-9	Q1		
Q10-15	Q4		
Q16-18	Q1		
Q19	Q4		
R1-3		4010222	R: COMP 2.2K
R4-6		4010151	R: COMP 150
R7-9		4010102	R: COMP 1K
R10	R1		
R11		4010681	R: COMP 680
R12	R1		
R13	R7		
R14	R4		
R15	R1		
R16		4010473	R: COMP 47K
R17	R1		
R18		4010272	R: COMP 2.7K
R19-20	R1		
R21	R18		
R22		4010103	R: COMP 10K
R23	R18		
R24		4010104	R: COMP 100K
R25-26	R1		
R27		4010101	R: COMP 100
R28		4010562	R: COMP 5.6K
R29	R27		
R30	R22		
R31		4010561	R: COMP 560
R32-33	R7		
R34	R28		
R35	R7		
R36	R11		
R37	R1		
R38	R28		
R39	R22		
R40	R28		
R41	R22		
R42-43	R28		
R44	R22		
R45	R28		
R46	R22		
R47-48	R28		
R49-51	R7		
R52	R11		
R53	R22		
R54	R31		
R55	R7		
R56		4010332	R: COMP 3.3K
R57-58	R1		
R59-60	R7		
R61-62	R22		
R63	R28		
R64	R1		
R65		4010182	R: COMP 1.8K
U1		3007404	IC: HEX INVERT
U2		3007405	IC: HEX INVERT
U3		3007408	IC: AND GT
U4	U1		
U5		3007432	IC: OR GT
U6		3008601	IC: ONE SHOT
U7		3007400	IC: NAND GT
U8	U6		
U9	U2		

TABLE 8-4. REPLACEABLE PARTS LIST

PCB ASSY A105 P/N: 2020009 CONTROL 1

REF	SAME	EIP P/N	DESCRIPTION
C1-2		2150003	C: CER .01 UF
C3		2300010	C: TANT 10 UF
C4-6	C1		
C7		2250001	C: MICA 10 PF
C8-11	C1		
C12	C7		
C13		2300015	C: TANT 33 UF
C14	C7		
C15	C1		
C16	C7		
C17-18	C1		
C19	C3		
C20	C1		
C21	C3		
C22	C1		
C23	C13		
C24	C1		
C25	C3		
J1		2630003	SOCKET: 14 PN
Q1		4704258	XSTR: PNP SW
Q2/4		4710014	XSTR: MTCH PR
Q3	Q1		
Q4	Q2		
Q5		4704126	XSTR: PNP GP
Q6-7		4704124	XSTR: NPN GP
R1		4010153	R: COMP 15K
R2		4010221	R: COMP 220
R3		4010680	R: COMP 68
R4		4010561	R: COMP 560
R5		4010101	R: COMP 100
R6		4010271	R: COMP 270
R7		4010331	R: COMP 330
R8		4010151	R: COMP 150
R9-11		4010471	R: COMP 470
R12	R7		
R13	R5		
R14	R7		
R15		4010821	R: COMP 820
R16		4010122	R: COMP 1.2K
R17		4010182	R: COMP 1.8K
R18-19		4010102	R: COMP 1K
R20		4010332	R: COMP 3.3K
R21	R15		
R22	R16		
R23	R20		
R24-25		4010391	R: COMP 390
R26		4010103	R: COMP 10K
R27	R4		
R28	R24		
R29	R20		
R30-31	R18		
R32		4010222	R: COMP 2.2K
R33	R20		
R34	R24		
R35	R15		
R36	R16		
R37	R18		
R38	R20		
R39	R18		
R40	R20		
R41-42	R18		
R43	R20		
R44	R15		
R45	R16		
R46	R20		
R47-49	R32		
R50	R26		
R51-52	R32		
R53	R15		
R54	R20		
R55	R18		
R56-57	R32		
U1		3008601	IC: ONE SHOT
U2		3007490	IC: DEC GT
U3		3007402	IC: NOR GT
U4		3110105	IC: OR GT
U5		3090002	IC: AND GT
U6		3007404	IC: HEX INVERT
U7	U2		
U8		3011039	IC: QUAD TRANS
U9	U2		
U10		3110131	IC: DUAL F/F
U11	U6		
U12		3074155	IC: DECODER
U13		3007432	IC: OR GT
U14		3007400	IC: NAND GT
U15-16	U2		
U17	U5		
U18	U1		
U19		3035009	IC: DIVIDER
U20	U6		
U21	U3		
U22		3007476	IC: DUAL F/F

PCB ASSY A106 P/N: 2020048 HIGH FREQ

REF	SAME	EIP P/N	DESCRIPTION
C1-2		2300015	C: TANT 33 UF
C3-4		2150003	C: CER .01 UF
C5		2160004	C: CER 10 PF
C6		2300010	C: TANT 10 UF
C7-8	C3		
C9		2150001	C: CER .001 UF
C10-11	C3		
C12		2259999	C: MICA S.A.T.
C13	C3		
C14	C6		
C15	C3		
C16	C6		
C17	C3		
C18	C1		
C19	C3		
C20		2150004	C: CER .1 UF
C21	C3		
C22		2250002	C: MICA 100 PF
C23	C9		

TABLE 8-4. REPLACEABLE PARTS LIST

REF	SAME	EIP P/N	DESCRIPTION
CR1-4		2710016	DI: HOT CARR
CR5		2704154	DI: GP
CR6		2710023	DI: TUNNEL
CR7	CR5		
CR8		2705234	DI: ZENER
CR9	CR1		
CR10	CR5		
CR11		2705230	DI: ZENER
CR12	CR5		
CR13	CR1		
CR14-16	CR5		
J1-2		2610018	CONN: JK
J3		2630003	SOCKET: 14 PN
J4	J1		
L1-8			P/O PCB
Q1		4704124	XSTR: NPN GP
Q2		4710011	XSTR: SELECT
Q3		4704959	XSTR: PNP RF
Q4-5		4710017	XSTR: NPN RF
Q6		4710010	XSTR: PNP RF
Q7		4710013	XSTR: SELECT
R1		4010510	R: COMP 51
R2		4130102	R: MT OX 1K
R3		4130120	R: MT OX 12
R4		4010221	R: COMP 220
R5	R3		
R6		4010392	R: COMP 3.9K
R7		4010202	R: COMP 2K
R8		4010331	R: COMP 330
R9	R2		
R10-11		4010102	R: COMP 1K
R12		4010302	R: COMP 3K
R13		4010272	R: COMP 2.7K
R14	R1		
R15	R12		
R16	R13		
R17		4010511	R: COMP 510
R18		4010596	R: COMP 5.6
R19	R1		
R20	R12		
R21	R13		
R22		4010471	R: COMP 470
R23		4130301	R: MT OX 300
R24		4130272	R: MT OX 2.7K
R25		4130821	R: MT OX 820
R26		4010101	R: COMP 100
R27		4130680	R: MT OX 68
R28	R18		
R29		4130430	R: MT OX 43
R30		4130560	R: MT OX 56
R31	R18		
R32	R30		
R33		4010112	R: COMP 1.1K
R34	R26		
R35		4010431	R: COMP 430
R36	R18		
R37		4010390	R: COMP 39
R38		4130470	R: MT OX 47
R39	R17		
R40		4010100	R: COMP 10
R41		4130390	R: MT OX 39
R42	R18		
R43		4130750	R: MT OX 75
R44		4130561	R: MT OX 560
R45		4130999	R: MTOX S.A.T.
R46	R35		
R47		4010151	R: COMP 150
R48			NOT USED
R49-51		4010103	R: COMP 10K
R52		4010681	R: COMP 680
R53	R49		
R54	R22		
U1-2		3043049	IC: AMPL
U3		3010637	IC: COUNTR

PCB ASSY A107 P/N: 2020011 POWER SUPPLY

REF	SAME	EIP P/N	DESCRIPTION
C1		2200010	C: ELEC 8.5K UF
C2		2300019	C: TANT 6.8 UF
C3		2250017	C: MICA 47 PF
C4	C2		
C5		2200005	C: ELEC 28K UF
C6	C2		
C7		2250002	C: MICA 100 PF
C8		2300016	C: TANT 47 UF
C9	C2		
C10		2300006	C: TANT 1.0 UF
C11		2150001	C: CER .001 UF
C12	C1		
C13	C2		
C14	C10		
C15	C11		
C16	C2		
C17		2200009	C: ELEC 8K UF
CR1-4		2704001	DI: RECT
CR5		2710028	DI: BRG RECT
CR6		2710008	DI: BRG RECT
CR7-8	CR1		
CR9		2720963	DI: ZENER
CR10-11	CR1		
CR12	CR9		
J1		2620006	CONN: 6 PIN
Q1		4710002	XSTR: PNP PWR
Q2		4705983	XSTR: NPN PWR
Q3	Q1		
Q4	Q2		
Q5		4704126	XSTR: PNP GP
Q6	Q1		
Q7	Q2		
Q8	Q5		
Q9	Q1		
Q10	Q2		

TABLE 8-4. REPLACEABLE PARTS LIST

REF	SAME	EIP P/N	DESCRIPTION
R1		4010680	R: COMP 68
R2		4010390	R: COMP 39
R3		4010751	R: COMP 750
R4		4110006	R: WW 0.33
R5	R3		
R6		4061472	R: MF 14.7K
R7		4250009	R: VAR 500
R8		4062261	R: MF 2.26K
R9		4020430	R: COMP 43
R10	R1		
R11		4010220	R: COMP 22
R12		4010151	R: COMP 150
R13		4110007	R: WW 0.2
R14		4065621	R: MF 5.62K
R15	R7		
R16		4062871	R: MF 2.87K
R17		4130123	R: MT OX 12K
R18		4020191	R: COMP 1.1
R19		4130162	R: COMP 1.6K
R20		4065761	R: MF 5.76K
R21		4250003	R: VAR 1K
R22		4062431	R: MF 2.43K
R23	R1		
R24		4010101	R: COMP 100
R25		4010102	R: COMP 1K
R26		4130512	R: MT OX 5.1K
R27	R18		
R28		4130911	R: MT OX 910
R29		4010911	R: COMP 910
R30	R22		
R31	R7		
R32	R22		
R33	R1		
R34	R24		
R35	R25		
U1-2		3040305	IC: VOLT REG
U3-4		3040304	IC: VOLT REG

PCB ASSY A108 P/N: 2020012 REF. OSC. BUFFER

REF	SAME	EIP P/N	DESCRIPTION
C1-21		2150003	C: CER .01 UF
CR1-5		2704154	DI: GP SW
J1		2630003	SOCKET: 14 PIN
J2		2620029	CONN: 3 PIN
J3		2620012	CONN: 9 PIN
J4		2620030	CONN: 4 PIN
Q1-4		4703563	XSTR: NPN
Q5		4704258	XSTR: PNP RF
Q6		4710011	XSTR: SELECT
Q7-8	Q1		
Q9	Q5		
Q10	Q1		
Q11	Q5		
Q12-13	Q1		
Q14	Q5		
Q15	Q1		
Q16	Q6		
Q17-18	Q1		
Q19	Q5		

PCB ASSY A108 P/N: 2020012 REF. OSC. BUFFER

REF	SAME	EIP P/N	DESCRIPTION
C1-21		2150003	C: CER .01 UF
CR1-5		2704154	DI: GP SW
J1		2630003	SOCKET: 14 PIN
J2		2620029	CONN: 3 PIN
J3		2620012	CONN: 9 PIN
J4		2620030	CONN: 4 PIN
Q1-4		4703563	XSTR: NPN
Q5		4704258	XSTR: PNP RF
Q6		4710011	XSTR: SELECT
Q7-8	Q1		
Q9	Q5		
Q10	Q1		
Q11	Q5		
Q12-13	Q1		
Q14	Q5		
Q15	Q1		
Q16	Q6		
Q17-18	Q1		
Q19	Q5		
R1		4010822	R: COMP 8.2K
R2		4010392	R: COMP 3.9K
R3		4010391	R: COMP 390
R4		4010681	R: COMP 680
R5		4010202	R: COMP 2K
R6	R1		
R7		4010222	R: COMP 2.2K
R8		4010751	R: COMP 750
R9	R5		
R10	R1		
R11		4010181	R: COMP 180
R12		4010270	R: COMP 27
R13		4010301	R: COMP 300
R14		4010100	R: COMP 10
R15	R1		
R16		4010432	R: COMP 4.3K
R17	R4		
R18		4010561	R: COMP 560
R19	R14		
R20		4010112	R: COMP 1.1K
R21-22		4010591	R: COMP 5.1
R23		4130103	R: MT OX 10K
R24		4130202	R: MT OX 2K
R25		4130621	R: MT OX 620
R26		4130999	R: MT OX S.A.T.
R27		4130431	R: MT OX 430
R28	R7		
R29		4010512	R: COMP 5.1K
R30	R1		

TABLE 8-4. REPLACEABLE PARTS LIST

REF	SAME	EIP P/N	DESCRIPTION
R31		4010362	R: COMP 3.6K
R32		4010621	R: COMP 620
R33		4010361	R: COMP 360
R34		4010431	R: COMP 430
R35		4130911	R: MT OX 910
R36	R7		
R37	R14		
R38	R1		
R39	R16		
R40	R4		
R41	R18		
R42	R14		
R43	R20		
R44-45	R21		
R46		4010999	R: COMP S.A.T.
U1		3007401	IC: NAND GT

PCB ASSY A109 P/N: 2020019 PRESCALER

REF	SAME	EIP P/N	DESCRIPTION
C1		2100005	C: CHIP 150 PF
C2-5		2100002	C: CHIP 1000 PF
C6-7		2250007	C: MICA 2 PF
C8-10	C2		
C11		2300015	C: TANT 33 UF
C12	C2		
C13-16		2150003	C: CER .01 UF
C17	C2		
C18-21	C13		
C22-23	C11		
C24-25	C13		
C26-27		2300010	C: TANT 10 UF
CR1-4		2710016	DI: HOT CARR
J1		2610018	CONN: JACK
L1		3510008	IND: .25 UH
P1		2040012	ASSY: CABLE
Q1		4710002	XSTR: PNP PWR
Q2		4704124	XSTR: NPN GP
Q3		4710003	XSTR: NPN PWR
Q4		4710010	XSTR: PNP RF
Q5/7		4710015	XSTR: MTCH PR
Q6	Q2		
Q7	Q5		
Q8	Q2		
Q9-12		4704126	XSTR: PNP GP
R1		4010221	R: COMP 220
R2		4010240	R: COMP 24
R3	R1		
R4		4010391	R: COMP 390
R5-6		4000151	R: COMP 150
R7		4000510	R: COMP 51
R8		4010184	R: COMP 180K
R9-10		4150390	R: MT OX 39
R11		4010100	R: COMP 10
R12		4010102	R: COMP 1K
R13		4010681	R: COMP 680
R14	R8		
R15-16		4051002	R: PREC 10K
R17		4010472	R: COMP 4.7K
R18		4010332	R: COMP 3.3K
R19		4010224	R: COMP 220K
R20		4010562	R: COMP 5.6K
R21-22		4010152	R: COMP 1.5K
R23		4010122	R: COMP 1.2K
R24		4000999	R: COMP S.A.T.
R25-26		4000220	R: COMP 22
R27	R12		
R28		4010999	R: COMP S.A.T.
R29		4010101	R: COMP 100
R30	R12		
R31-32	R13		
R33		4010103	R: COMP 10K
R34		4010222	R: COMP 2.2K
R35	R1		
R36		4010331	R: COMP 330
R37	R12		
R38-39	R21		
R40	R33		
R41		4250003	R: VAR 1K
R42	R18		
R43	R12		
R44	R33		
R45	R20		
R46		4010243	R: COMP 24K
R47	R33		
R48		4010999	R: COMP S.A.T.
U1		3040417	IC: AMPL
U2		3010615	IC: CNTR/DIVDR
U3-4		3040741	IC: OP AMPL

PCB ASSY A110 P/N: 2020004 DISPLAY

REF	SAME	EIP P/N	DESCRIPTION
DS1-11		2800004	LED: NUM IND
DS12-15		2800001	LED: IND
J1-2		2040001	ASSY: CABLE
P1		2040013	ASSY: HARNESS
Q1-7		4710019	XSTR: PNP GP
R1		4010471	R: COMP 470
R2		4010122	R: COMP 1.2K
R3	R1		
R4	R2		
R5	R1		
R6	R2		
R7	R1		
R8	R2		
R9		4010331	R: COMP 330
R10	R2		
R11		4010681	R: COMP 680

REF	SAME	EIP P/N	DESCRIPTION
R12	R2		
R13	R11		
R14	R9		
R15	R2		

PCB ASSY A111 P/N: 2020046 PREAMPLIFIER

REF	SAME	EIP P/N	DESCRIPTION
C1		2250018	C: MICA 470 PF
C2		2150003	C: CER .01 UF
C3		2250012	C: MICA 27 PF
C4		2300017	C: TANT 47 UF
C5		2300010	C: TANT 10 UF
C6	C2		
C7		2300022	C: TANT 22 UF
C8-9		2300015	C: TANT 33 UF
C10-11	C2		
C12		2160013	C: CER 4.7 PF
CR1		2705236	DI: ZENER
CR2-5		2704154	DI: GP
CR6-9		2710016	DI: HOT CARR
CR10	CR2		
CR11		2705239	DI: ZENER
FL1-3		2350017	C: RF FLTR
J1		2620027	CONN: JK
J2		2610018	CONN: JK
K1		3900003	RLY: SIGNAL
L1-3			P/O PCB
Q1		4704126	XSTR: PNP GP
Q2		4704416	XSTR: J-FET
Q3		4710012	XSTR: SELECT
Q4		4710010	XSTR: PNP RF
R1		4010510	R: COMP 51
R2		4020510	R: COMP 51
R3		4000105	R: COMP 1M
R4		4010202	R: COMP 2K
R5		4010182	R: COMP 1.8K
R6		4010105	R: COMP 1M
R7		4010512	R: COMP 5.1K
R8		4010682	R: COMP 6.8K
R9		4010100	R: COMP 10
R10		4010472	R: COMP 4.7K
R11	R1		
R12		4010181	R: COMP 180
R13		4010121	R: COMP 120
R14		4010821	R: COMP 820
R15	R5		
R16	R14		
R17		4130102	R: MT OX 1K
R18		4130120	R: MT OX 12
R19		4010221	R: COMP 220
R20	R18		
R21		4010331	R: COMP 330
R22-23		4010102	R: COMP 1K
R24	R17		
R25		4130910	R: MT OX 91
R26		4010596	R: COMP 5.6
R27		4130101	R: MT OX 100
R28-29	R22		
R30		4010511	R: COMP 510
U1		3043049	IC: AMPL

PCB ASSY A113 P/N: 2020038 CNTR INTERCONN

REF	SAME	EIP P/N	DESCRIPTION
C1		2250011	C: MICA 220 PF
C2		2300015	C: TANT 33 UF
CR1-7		2704154	DI: GP
J1			NOT USED
J2		2620014	CONN: 4 PIN
J3		2620044	CONN: 12 PIN
J4		2620047	CONN: 5 PIN
J5		2620016	CONN: 6 PIN
J6	J4		
J7-8		2630009	SOCKET: 14 PIN
J9	J2		
J10	J4		
Q1		4704124	XSTR: NPN GP
R1/S9		4290001	(SMPL RATE)
R2		4010100	R: COMP 10
R3		4010151	R: COMP 150
R4-5			NOT USED
R6		4010750	R: COMP 75
R7-8		4010222	R: COMP 2.2K
R9-13			NOT USED
R14	R6		
R15		4010332	R: COMP 3.3K
R16		4010182	R: COMP 1.8K
S1-8		4500007	SW: PB 8 STA

ASSY A116 P/N: 2030002 TCXO: 10 MHz

ASSY A2 (CONVERTER CHASSIS COMPONENTS)

REF	SAME	EIP P/N	DESCRIPTION
A2Q1		4710009	XSTR: PNP PWR

TABLE 8-4. REPLACEABLE PARTS LIST

PCB ASSY A201		P/N: 2020091	SOURCE/AMPL
REF	SAME	EIP P/N	DESCRIPTION
C1-2		2150003	C: CER .01 UF
C3		2300008	C: TANT 1 UF
C4		2300015	C: TANT 33 UF
C5-10	C1		
C11		2160016	C: CER 20 PF
C12		2160007	C: CER 18 PF
C13-15	C1		
C16		2350003	C: TRIM 8-25 PF
C17		2160013	C: CER 4.7 PF
C18		2160006	C: CER 15 PF
C19	C1		
C20		2250005	C: MICA 150 PF
C21	C1		
C22		2160005	C: CER 12 PF
C23		2350001	C: TRIM 2-8 PF
C24		2160008	C: CER 2.2 PF
C25		2160004	C: CER 10 PF
C26-28	C1		
C29-30	C22		
C31	C11		
C32	C1		
C33-34		2150001	C: CER .001 UF
C35	C16		
C36	C17		
C37	C18		
C38	C1		
C39		2250002	C: MICA 100 PF
C40		2350002	C: TRIM 5.5-18PF
C41-42		2160010	C: CER 24 PF
C43-44	C1		
C45	C40		
C46	C41		
C47-49	C1		
C50	C39		
C51	C1		
C52	C40		
C53	C41		
C54-55	C1		
C56		2350022	C: TRIM 5.5-18PF
C57-58	C39		
C59-61	C1		
C62		2300010	C: TANT 10 UF
C63		2159999	C: CER S.A.T.
C64-66	C1		
C67		2250014	C: MICA 33 PF
C68			NOT USED
C69-79	C1		
CR1		2710006	DI: HOT CARR
CR2		2704154	DI: GP
CR3		2710012	DI: VARICAP
CR4	CR2		
CR5	CR1		
CR6-10	CR2		
L1-2			NOT USED
L3		3520007	IND: 100 UH
L4		3510003	IND: 1 UH
L5-6			P/O PCB
L7	L4		
L8-9			P/O PCB
L10		3510010	IND: 1.2 UH
L11		3510001	IND: .1 UH
L12	L4		
L13			P/O PCB
L14-15	L10		
L16	L4		
L17			P/O PCB
L18-21	L10		
L22		3510011	IND: .12 UH
L23	L4		
L24-33	L10		
Q1-2		4704124	XSTR: NPN GP
Q3		4710012	XSTR: SELECT
Q4		4710010	XSTR: PNP RF
Q5	Q3		
Q6-7		4704416	XSTR: J-FET
Q8	Q3		
Q9	Q4		
Q10		4704126	XSTR: PNP GP
Q11		4710013	XSTR: SELECT
Q12	Q6		
Q13-14	Q3		
Q15-16		4720002	XSTR: NPN RF
Q17		4710003	XSTR: NPN PWR
Q18-21	Q10		
Q22	Q1		
R1		4010202	R: COMP 2K
R2		4010510	R: COMP 51
R3		4130682	R: MT OX 6.8K
R4		4130392	R: MT OX 3.9K
R5		4130271	R: MT OX 270
R6		4130202	R: MT OX 2K
R7	R4		
R8	R3		
R9-11		4010511	R: COMP 510
R12		4010391	R: COMP 390
R13		4010111	R: COMP 110
R14	R5		
R15		4130182	R: MT OX 1.8K
R16		4130122	R: MT OX 1.2K
R17-18		4130622	R: MT OX 6.2K
R19		4130562	R: MT OX 5.6K
R20		4130912	R: MT OX 9.1K
R21		4130302	R: MT OX 3K
R22	R16		
R23		4130821	R: MT OX 820
R24		4130102	R: MT OX 1K
R25		4010102	R: COMP 1K
R26		4010472	R: COMP 4.7K
R27		4130511	R: MT OX 510
R28		4130221	R: MT OX 220
R29	R27		
R30	R15		
R31	R28		
R32		4130332	R: MT OX 3.3K
R33		4130243	R: MT OX 24K
R34		4010243	R: COMP 24K
R35	R33		
R36	R24		

REF	SAME	EIP P/N	DESCRIPTION
R37		4130113	R: MT OX 11K
R38		4010393	R: COMP 39K
R39		4130201	R: MT OX 200
R40	R24		
R41	R20		
R42	R21		
R43	R16		
R44	R23		
R45	R24		
R46	R4		
R47	R21		
R48	R39		
R49		4130300	R: MT OX 30
R50		4130999	R: MT OX S.A.T.
R51	R17		
R52	R24		
R53	R33		
R54			NOT USED
R55		4010561	R: COMP 560
R56	R2		
R57-58	R17		
R59	R24		
R60		4130223	R: MT OX 22K
R61	R24		
R62		4130103	R: MT OX 10K
R63	R37		
R64	R23		
R65		4130272	R: MT OX 2.7K
R66		4010272	R: COMP 2.7K
R67		4130472	R: MT OX 4.7K
R68		4130391	R: MT OX 390
R69	R32		
R70		4010101	R: COMP 100
R71		4010103	R: COMP 10K
R72-78	R70		
U1		3112000	IC: TRNSLTR
U2		3110138	IC: CNTR
U3		3014044	IC: DETECTR
U4-5		3040741	IC: OP AMPL

PCB ASSY A202		P/N: 2020029	CNV CNTRL 2
REF	SAME	EIP P/N	DESCRIPTION
C1-2		2150003	C: CER .01 UF
C3		2300020	C: TANT .15 UF
C4		2150001	C: CER .001 UF
C5 6	C1		
C7		2300006	C: TANT 1.0 UF
C8-9	C1		
C10	C4		
C11		2350004	C: CER .0015 UF
C12	C1		
C13		2150008	C: CER .005 UF
CR1		2720827	DI: ZENER
CR2		2704154	DI: GP
CR3		2704757	DI: ZENER
CR4		2704001	DI: RECT
CR5	CR2		

REF	SAME	EIP P/N	DESCRIPTION
J1-2		2630003	SOCKET: 14 PIN
J3		2620031	CONN: 7 PIN
Q1-11		4703641	XSTR: NPN SW
Q12		4704124	XSTR: NPN GP
Q13		4710018	XSTR: PNP
Q14		4704126	XSTR: PNP GP
Q15		4710005	XSTR: UNI JCT
Q16-17	Q12		
R1-2		4140035	R: PREC 8K
R3		4057500	R: PREC 750
R4		4250006	R: VAR 10K
R5		4052003	R: PREC 200K
R6-7		4010226	R: COMP 22M
R8		4010186	R: COMP 18M
R9		4010272	R: COMP 2.7K
R10-11		4010166	R: COMP 16M
R12	R9		
R13	R10		
R14	R9		
R15		4010825	R: COMP 8.2M
R16	R9		
R17		4010625	R: COMP 6.2M
R18	R9		
R19		4010305	R: COMP 3M
R20-21	R9		
R22		4101004	R: PREC 1M
R23		4010103	R: COMP 10K
R24	R9		
R25		4105003	R: PREC 500K
R26	R23		
R27	R9		
R28		4104003	R: PREC 400K
R29	R23		
R30	R9		
R31		4102003	R: PREC 200K
R32	R23		
R33	R9		
R34		4101003	R: PREC 100K
R35	R23		
R36	R9		
R37		4108002	R: PREC 80K
R38	R23		
R39	R9		
R40		4140033	R: PREC 40K
R41		4010123	R: COMP 12K
R42	R9		
R43		4140032	R: PREC 20K
R44		4010203	R: COMP 20K
R45	R9		
R46		4140031	R: PREC 10K
R47		4010222	R: COMP 2.2K
R48		4140030	R: PREC 8K
R49		4010122	R: COMP 1.2K
R50		4140029	R: PREC 4K
R51-52		4010596	R: COMP 5.6
R53			NOT USED
R54	R51		
R55		4140034	R: PREC 3K
R56		4010152	R: COMP 1.5K
R57		4054992	R: PREC 49.9K

TABLE 8-4. REPLACEABLE PARTS LIST

REF	SAME	EIP P/N	DESCRIPTION
R58		4140039	R: PREC 3.7K
R59		4010162	R: COMP 1.6K
R60		4280009	R: VAR 500
R61		4110003	R: WW 5
R62		4250005	R: VAR 5K
R63		4053922	R: PREC 39.2K
R64	R55		
R65	R57		
R66-67		4010391	R: COMP 390
R68		4010102	R: COMP 1K
R69	R23		
R70	R41		
R71		4010332	R: COMP 3.3K
R72	R51		
R73		4010120	R: COMP 12
R74		4010221	R: COMP 220
R75		4010999	R: COMP S.A.T.
R76		4010621	R: COMP 620
R77		4010242	R: COMP 2.4K
R78		4000202	R: COMP 2K
R79		4010472	R: COMP 4.7K
R80		4010999	R: COMP S.A.T.
R81	R79		
R82		4010999	R: COMP S.A.T.
R83	R62		
R84		4052002	R: PREC 20K
R85	R62		
R86	R84		
R87	R62		
R88	R84		
R89	R62		
R90	R84		
R91	R62		
R92		4051622	R: PREC 16.2K
R93	R62		
R94	R92		
R95	R62		
R96	R84		
R97	R62		
R98	R84		
R99	R44		
R100		4051002	R: PREC 10.0K
R101		4051212	R: PREC 12.1K
R102		4051912	R: PREC 19.1K
R103		4051501	R: PREC 1.5K
R104-106		4010202	R: COMP 2K
R107-108		4010564	R: COMP 560K
U1-3		3040741	IC: OP AMPL
U4		3090003	IC: AND GT
U5-6		3007490	IC: DEC CNTR
U7		3007404	IC: HEX INVERT
U8		3074176	IC: DEC CNTR
U9	U7		
U10	U8		
U11	U4		
U12	U8		
U13		3007400	IC: NAND GT
U14		3007402	IC: NOR GT
U15		3007408	IC: AND GT
U16		3007442	IC: DECODER
U17-18	U1		

PCB ASSY A203 P/N: 2020016 CONV CONTRL 1

REF	SAME	EIP P/N	DESCRIPTION
C1		2150003	C: CER .01 UF
C2-5		2150001	C: CER .001 UF
C6	C1		
C7	C2		
C8-9		2250006	C: MICA 180 PF
C10		2160006	C: CER 15 PF
C11	C1		
C12		2160014	C: CER 6.8 PF
C13	C2		
C14-17	C1		
C18	C2		
C19		2160010	C: CER 24 PF
C20-21	C2		
C22-23	C1		
C24-25	C2		
C26	C1		
C27	C2		
C28		2250018	C: MICA 470 PF
C29		2150005	C: CER .002 UF
C30		2350015	C: MF .047 UF
C31-32	C1		
C33		2300005	C: TANT .47 UF
C34	C2		
C35		2150008	C: CER .005 UF
C36-38	C1		
C39		2300003	C: TANT .15 UF
C40	C1		
C41-42		2300008	C: TANT 1 UF
C43	C1		
C44	C41		
C45-46	C1		
CR1		2704154	DI: GP
CR2		2705237	DI: ZENER
CR3	CR1		
CR4/5		2710014	DI: MTCH PR
CR6-7	CR1		
CR8/9	CR4/5		
CR10	CR1		
CR11		2710013	DI: LO-LKGE
L1		3510001	IND: .1 UH
L2-3			P/O PCB
L4		3510004	IND: .22 UH
L5-7			P/O PCB
L8		3510003	IND: 1 UH
P1			P/O PCB
P2		2040010	ASSY: CABLE
P3		2040011	ASSY: CABLE
Q1-2		4710012	XSTR: SELECT
Q3		4710010	XSTR: PNP RF
Q4		4710017	XSTR: NPN SW
Q5	Q1		
R1		4010511	R: COMP 510
R2		4010820	R: COMP 82
R3		4010201	R: COMP 200

REF	SAME	EIP P/N	DESCRIPTION
R4-5		4010222	R: COMP 2.2K
R6		4010270	R: COMP 27
R7		4010102	R: COMP 1K
R8	R4		
R9		4010751	R: COMP 750
R10		4010510	R: COMP 51
R11		4010131	R: COMP 130
R12	R10		
R13		4010331	R: COMP 330
R14	R7		
R15	R4		
R16	R9		
R17		4010111	R: COMP 110
R18	R13		
R19	R17		
R20	R10		
R21		4250001	R: VAR 100
R22-23		4010184	R: COMP 180K
R24		4010223	R: COMP 22K
R25		4010562	R: COMP 5.6K
R26		4010622	R: COMP 6.2K
R27		4010332	R: COMP 3.3K
R28		4010151	R: COMP 150
R29		4010272	R: COMP 2.7K
R30		4010101	R: COMP 100
R31	R1		
R32	R6		
R33		4010750	R: COMP 75
R34-35	R22		
R36-37		4051002	R: PREC 10K
R38	R33		
R39	R27		
R40	R26		
R41		4250006	R: VAR 10K
R42	R4		
R43		4010330	R: COMP 33
R44	R7		
R45	R28		
R46	R17		
R47		4010271	R: COMP 270
R48	R17		
R49	R7		
R50	R13		
R51		4010153	R: COMP 15K
R52	R7		
R53	R41		
R54	R7		
R55	R3		
R56		4010182	R: COMP 1.8K
R57	R51		
R58		4010913	R: COMP 91K
R59		4010103	R: COMP 10K
R60		4010472	R: COMP 4.7K
R61		4010152	R: COMP 1.5K
R62	R60		
R63	R7		
R64		4010113	R: COMP 11K
R65		4010100	R: COMP 10
R66	R47		
R67		4010104	R: COMP 100K
R68		4010174	R: COMP 470K
R69	R60		
R70-71	R59		
R72	R4		
R73	R51		
R74	R59		
R75		4010303	R: COMP 30K
U1		3043049	IC: DIFF AMPL
U2		3040741	IC: OP AMPL
U3		3041741	IC: OP AMPL
U4	U2		
U5		3048007	IC: OP AMPL
U6	U2		
U7-8		3011414	IC: DIFF COMP
U9		3007408	IC: AND GT
U10		3007400	IC: NAND GT
U11		3007473	IC: DUAL F/F
U12		3074123	IC: RETRIG MV
U13		3008601	IC: ONE SHOT
U14-15	U11		
U16	U9		
U17	U11		
U18		3007405	IC: HEX INVERT
U19	U13		

PCB ASSY A204 P/N: 2020014 VIDEO AMPL

REF	SAME	EIP P/N	DESCRIPTION
C1		2150003	C: CER .01 UF
C2		5280013-01	C: MODIFIED
C3	C1		
C4-5		2169999	C: CER S.A.T.
C6		2150001	C: CER .001 UF
C7	C1		
C8-9	C6		
C10	C1		
C11		2169999	C: CER S.A.T.
C12-13	C1		
C14-15	C6		
C16	C1		
C17		2169999	C: CER S.A.T.
C18	C6		
C19-20	C1		
C21	C6		
C22	C1		
C23		2160015	C: CER 8.2 PF
C24	C6		
C25	C1		
C26	C6		
C27	C1		
C28		2169999	C: CER S.A.T.
C29	C1		
C30-31	C6		
C32	C1		
C33		2160008	C: CER 2.2 PF
C34		2169999	C: CER S.A.T.
C35-36		2250013	C: MICA 300 PF
C37-38	C1		
C39-40		2300010	C: TANT 10 UF
C41		2250009	C: MICA 200 PF
C42-44	C1		
C45			NOT USED

TABLE 8-4. REPLACEABLE PARTS LIST

REF	SAME	EIP P/N	DESCRIPTION
C46-47		2150005	C: CER .002 UF
C48	C6		
C49-50	C1		
C51		2300008	C: TANT 1 UF
C52	C6		
C53-54	C1		
C55	C46		
C56-57	C1		
C58			NOT USED
C59		2250018	C: MICA 470 PF
C60	C39		
C61	C1		
C62	C39		
C63			NOT USED
C64		2169999	C: CER S.A.T.
CR1-2		2704154	DI: GP
CR3-5		2710024	DI: PIN
CR6		2710022	DI: PIN
CR7-10	C1		
CR11	CR3		
CR12-16	CR1		
CR17			NOT USED
CR18-22	CR1		
CR23-24		2710004	DI: HOT CARR
CR25	CR1		
FL1-3		2350017	C: FDTH/FLTR
FL4		5000104	TERM: INSUL
J1		2610017	CONN: PC PLUG
J2-3		2610010	CONN: JK
L1		3510001	IND: .1 UH
L2		3510010	IND: .68 UH
L3		3510005	IND: 2.2 UH
P1		2040019	ASSY: HARNESS
Q1		4710013	XSTR: SELECT
Q2		4710010	XSTR: PNP RF
Q3		4710012	XSTR: SELECT
Q4	Q1		
Q5	Q2		
Q6	Q3		
Q7	Q1		
Q8	Q2		
Q9	Q3		
Q10	Q1		
Q11	Q2		
Q12	Q3		
Q13	Q1		
Q14-15	Q2		
Q16	Q1		
Q17-18	Q2		
Q19		4704124	XSTR: NPN GP
Q20		4710011	XSTR: SELECT
Q21-23	Q19		

REF	SAME	EIP P/N	DESCRIPTION
R1		4010151	R: COMP 150
R2		4010432	R: COMP 4.3K
R3		4010561	R: COMP 560
R4		4010271	R: COMP 270
R5		4010390	R: COMP 39
R6		4010180	R: COMP 18
R7		4010101	R: COMP 100
R8		4010360	R: COMP 36
R9		4010511	R: COMP 510
R10	R5		
R11	R7		
R12	R2		
R13	R3		
R14	R4		
R15	R5		
R16	R6		
R17	R7		
R18	R8		
R19	R9		
R20	R5		
R21		4010510	R: COMP 51
R22	R2		
R23	R3		
R24	R4		
R25		4010470	R: COMP 47
R26	R5		
R27	R6		
R28	R7		
R29	R8		
R30	R9		
R31	R21		
R32	R2		
R33	R3		
R34	R4		
R35	R5		
R36	R6		
R37	R7		
R38	R8		
R39	R9		
R40	R5		
R41	R21		
R42	R2		
R43	R3		
R44	R4		
R45	R5		
R46	R6		
R47		4010999	R: COMP S.A.T.
R48	R8		
R49		4010122	R: COMP 1.2K
R50		4010750	R: COMP 75
R51	R2		
R52	R3		
R53	R4		
R54	R5		
R55	R6		
R56	R7		
R57	R8		
R58	R49		

TABLE 8-4. REPLACEABLE PARTS LIST

REF	SAME	EIP P/N	DESCRIPTION
R59		4010243	R: COMP 24K
R60		4010153	R: COMP 15K
R61	R49		
R62		4010473	R: COMP 47K
R63		4010912	R: COMP 9.1K
R64		4010272	R: COMP 2.7K
R65		4010181	R: COMP 180
R66-67			NOT USED
R68	R65		
R69	R62		
R70	R65		
R71		4010222	R: COMP 2.2K
R72		4010226	R: COMP 22M
R73		4010102	R: COMP 1K
R74			NOT USED
R75		4010103	R: COMP 10K
R76		4010132	R: COMP 1.3K
R77		4010113	R: COMP 11K
R78		4010242	R: COMP 2.4K
R79		4010472	R: COMP 4.7K
R80	R9		
R81	R4		
R82		4010622	R: COMP 6.2K
R83		4010270	R: COMP 27
R84		4010201	R: COMP 200
R85		4010152	R: COMP 1.5K
R86	R21		
R87	R71		
R88	R75		
R89		4010682	R: COMP 6.8K
R90	R62		
U1-4		3040741	IC: OP AMPL

ASSY A205	2010007	MIXER

ASSY A206	2030003	ATTN/CONN

ASSY A207	2010097-01	COMB GN (350D)
ASSY A207	2010097-02	COMB GN (351D)

PCB ASSY A208 P/N: 2020025 CONV INTERCONN

REF	SAME	EIP P/N	DESCRIPTION
J1		2620042	CONN: 9 PIN
J2		2040027	ASSY: HARNESS
J3		2620014	CONN: 4 PIN

PROGRAMMING OPTIONS 01, 06, 07 (NOTE: THIS BOARD IS USED FOR THREE OPTIONS — PARTS USAGE WILL VARY ACCORDINGLY. CERTAIN COUNTERS USE ALTERNATE OPTION 06 AND 07 PC BOARDS.)

PCB ASSY A115 P/N: 2020035 PROGRAMMING

REF	SAME	EIP P/N	DESCRIPTION
C1		2150003	C: CER .01 UF
C2		2300015	C: TANT 33 UF
C3-6	C1		
J1-5		2630003	SOCKET: 14 PN
P1		2640004	CONN: 50 PIN
R1		4010151	R: COMP 150
U1-2		3007405	IC: HEX INVERT
U3		3007402	IC: QUAD GT
U4-5	U1		
U6	U3		
U7	U1		
U8	U3		
U9-12	U1		

OPTION 02 - YIG PRESET - THUMBWHEEL

REF	SAME	EIP P/N	DESCRIPTION
		4540002	SW: THMBWHL

OPTIONS 03, 04, 05: OVENIZED OSC (A112/A114)

REF	SAME	EIP P/N	DESCRIPTION
OPT 03		2030001-01	OSC: 5x10-9
OPT 04		2030001-02	OSC: 1x10-9
OPT 05		2030001-03	OSC: 5x10-10
A112R1		4260001	(T/B ADJ)
(OSC P/S)		2040009	ASSY: CABLE

PCB ASSY A114 P/N: 2020022 OVEN OSC P/S

REF	SAME	EIP P/N	DESCRIPTION
C1		2200001	C: ELEC 1250 UF
C2		2300010	C: TANT 10 UF
C3		2250017	C: MICA 47 PF
C4		2300008	C: TANT 1 UF
CR1		2710019	DI: BRDG RECT
CR2-3		2704001	DI: RECT
Q1		4710007	XSTR: NPN PWR

REF	SAME	EIP P/N	DESCRIPTION
R1		4110004	R: WW .5
R2		4062152	R: MF 21.5K
R3		4250009	R: VAR 500
R4		4061101	R: MF 1.1K
T1		4900002	XFMR: PWR
U1		3040305	IC: VOLT REG

OPTION 06: PGRM OFFSET (ALT PCB ASSY)

PCB ASSY A100 P/N: 2020033 OFFSET

REF	SAME	EIP P/N	DESCRIPTION
C1		2300015	C: TANT 33 UF
C2-4		2150003	C: CER .01 UF
J1		2630003	SOCKET: 14 PN
Q1		4704124	XSTR: NPN GP
R1-3		4010222	R: COMP 2.2K
U1		3007402	IC: NOR GT
U2		3007404	IC: HEX INVERT
U3-4		3007476	IC: DUAL F/F
U5		3007408	IC: AND GT
U6-8		3074192	IC: CLOCK

OPTION 07: REM PGRM (ALT PCB ASSY)

PCB ASSY A115 P/N: 2020027 REM PGRM

REF	SAME	EIP P/N	DESCRIPTION
C1-3		2150003	C: CER .01 UF
J1-2		2630003	SOCKET: 14 PN
J3		2640004	CONN: 50 PIN
R1		4010151	R: COMP 150
U1		3007405	IC: HEX INVERT
U2-4		3007402	IC: NOR GT
U5-8	U1		

OPTION 09: BCD OUTPUT

PCB ASSY A117 P/N: 2020039 BCD OUTPUT

REF	SAME	EIP P/N	DESCRIPTION
C1-2		2150003	C: CER .01 UF
C3		2300015	C: TANT 33 UF
C4	C1		
CR1		2704154	DI: GP
J1-3		2630003	SOCKET: 14 PN
J4		2620014	CONN: 4 PIN
P1		2640004	CONN: 50 PIN
Q1		4704401	XSTR: NPN
R1		4010220	R: COMP 22
R2-3		4010103	R: COMP 10K
U1-8		3000937	IC: HEX INVERT

SECTION 9

CIRCUIT SCHEMATICS & DESCRIPTIONS

COMPONENT LOCATORS

9-1. GENERAL

9-2. Schematics and Component Locators are arranged by Assembly number (A101, A102, etc.). Circuit descriptions and circuit theory are shown on the same or adjacent pages. All assembly related drawings and diagrams have the same figure number, but have different suffix letters (9-6A, 9-6B, etc.).

9-3. Parts Lists and Ordering Information will be found in Section 8.

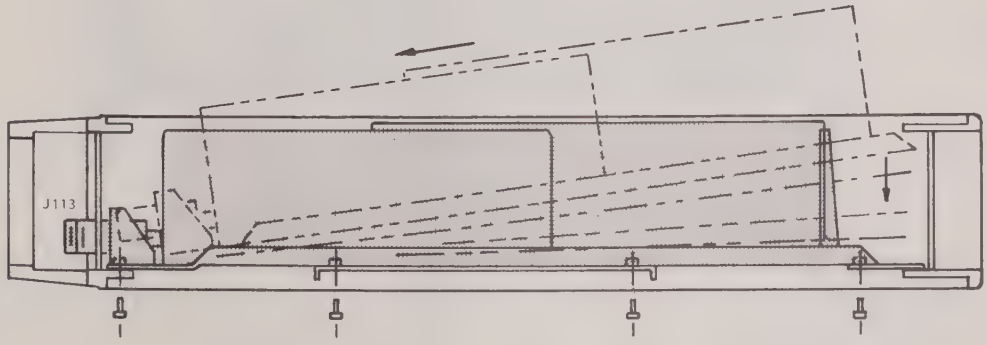
9-4. Unless otherwise specified, the following notes apply to all figures in this section.

a. Resistance values in ohms.

b. Capacitance values in microfarads ("pf" values in picofarads).

c. Connector reference numbers may not appear on part.

d. SAT = Selected at Test. Nominal value shown; part may not be installed. MP = Matched Pair.



FIELD INSTALLATION OF CONVERTER ASSEMBLY

1 WITH TOP AND BOTTOM COVERS REMOVED FROM BASIC COUNTER, LOWER CONVERTER INTO POSITION AS SHOWN IN DIAGRAM. TILT J113 DOWN AND FORWARD THROUGH HOLE IN FRONT PANEL.
2. INSTALL SIX 6-32 SCREWS FROM BOTTOM SIDE OF COUNTER INTO CAPTIVE NUTS ON CONVERTER. ALIGN J113 CONCENTRICALLY WITH FRONT PANEL HOLE; TIGHTEN SCREWS.
3 PLUG CABLES W16, W17, AND W18 INTO MATING CONNECTORS ON BASIC COUNTER (SEE CABLE INTER CONNECTION GUIDE); REPLACE COVERS. REVERSE ABOVE PROCEDURE TO REMOVE CONVERTER.

FIELD INSTALLATION OF PRESCALER ASSEMBLY

1 WITH TOP COVER REMOVED, PLUG PRESCALER (A109) INTO A113-XA109. MOUNT J112 IN FRONT PANEL HOLE.
2 PLUG CABLES W7 AND W11 INTO MATING CONNECTORS PROVIDED ON MODULES (SEE CABLE INTERCONNECTION GUIDE); REPLACE COVER.

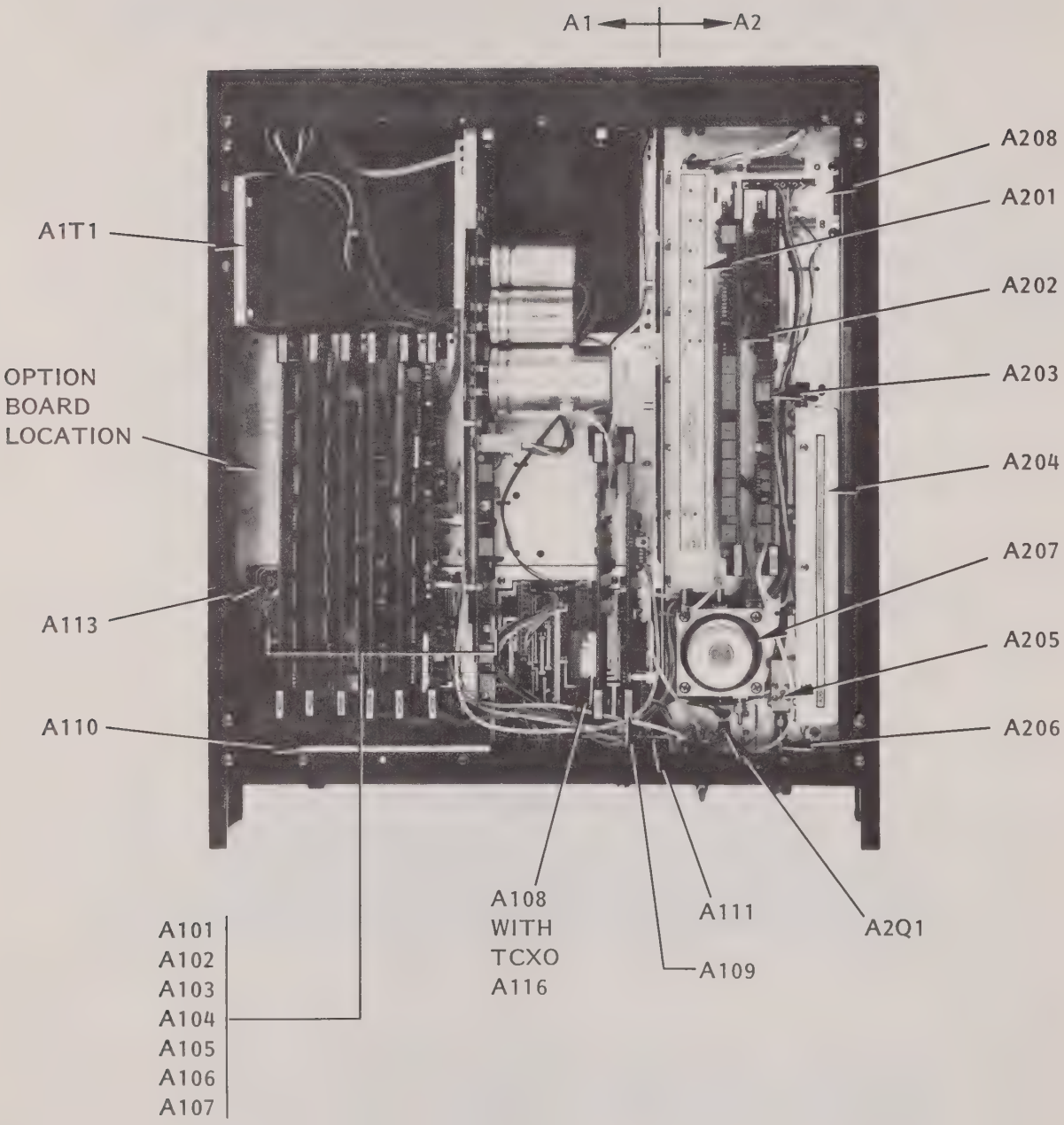
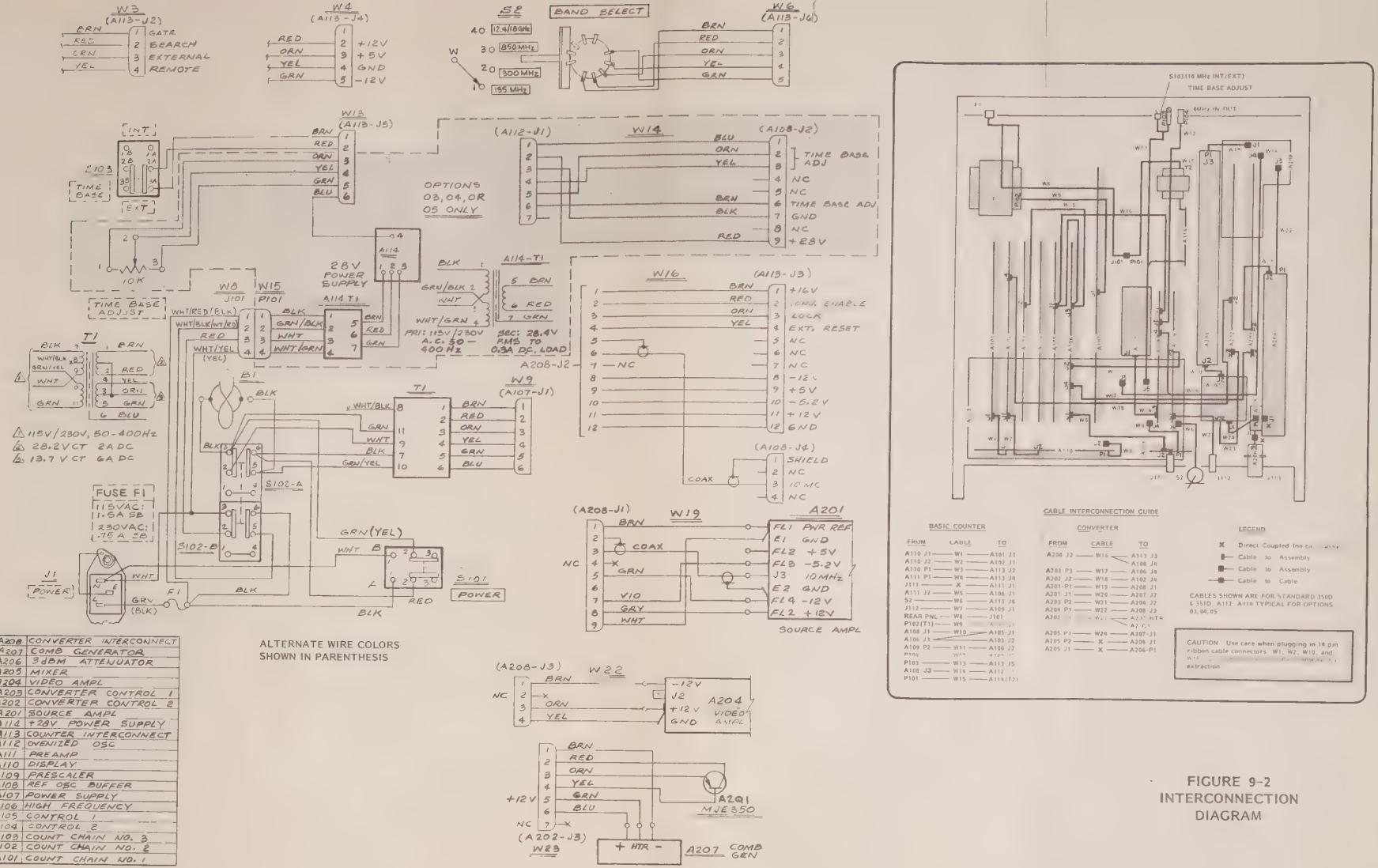


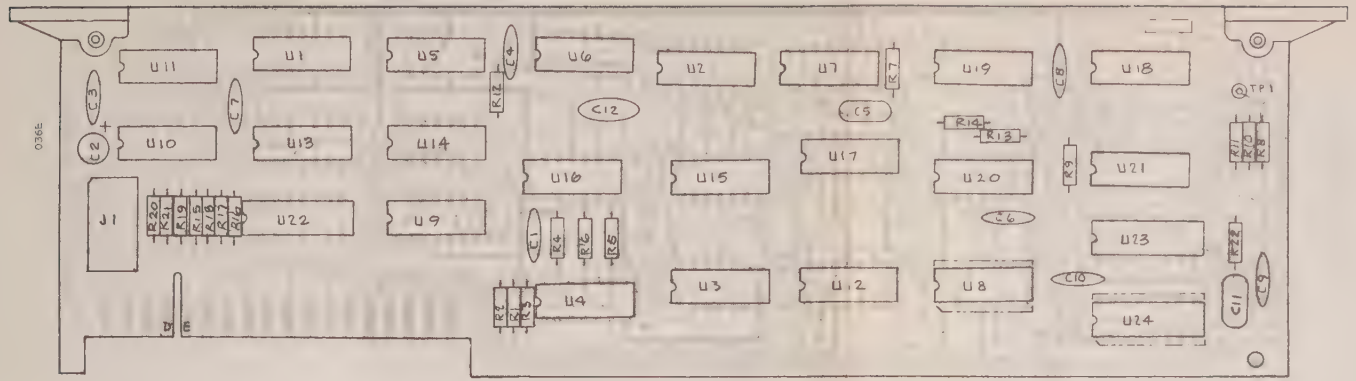
FIGURE 9-1
ASSEMBLY
LOCATOR



A208	CONVERTER INTERCONNECT
A207	COMB GENERATOR
A206	3dBM ATTENUATOR
A205	MIXER
A204	VIDEO AMPL
A203	CONVERTER CONTROL 1
A202	CONVERTER CONTROL 2
A201	SOURCE AMPL
A114	+28V POWER SUPPLY
A113	COUNTER INTERCONNECT
A112	OVENIZED OSC
A111	PREAMP
A110	DISPLAY
A109	PRESCALER
A108	REF OSC BUFFER
A107	POWER SUPPLY
A106	HIGH FREQUENCY
A105	CONTROL 1
A104	CONTROL 2
A103	COUNT CHAIN NO. 3
A102	COUNT CHAIN NO. 2
A101	COUNT CHAIN NO. 1

ALTERNATE WIRE COLORS SHOWN IN PARENTHESIS

FIGURE 9-2
INTERCONNECTION
DIAGRAM



GATE TIME	÷5 COUNT	B	C	D
1 sec.	5	0	0	0
100 ms.	4	0	0	1
10 ms.	3	1	1	0
1 ms	2	0	1	0
	1	1	0	0
	0	0	0	0

TABLE 9-3B
U15 PRESETS

COUNT CHAIN 1, 2, AND 3

Count Chain Boards 1, 2, and 3 (A101, A102, and A103) perform most of the actual frequency counting functions of the direct counter. The main components are: (1) a counting chain, (2) a storage unit, and (3) the display multiplexer.

The counting chain consists of a string of ten cascaded decimal counting units (DCUs), preceded by a quinary (÷5) counting unit. The quinary counter is sufficiently fast to follow the output of the binary (÷2) counter in the High Frequency Board, forming the first DCU. The remaining DCUs are each a standard integrated circuit having four output lines to indicate the state of the counter at any given time.

The storage unit is a string of quad latches, one for each of the eleven DCUs of the counting chain. An enable signal to the storage unit causes it to load the information from the DCUs.

The display multiplexer processes the information held in the eleven elements of the storage unit. The output of the storage unit is converted to the seven line code needed to drive the seven segments of each display digit. Power is applied to each digit sequentially for 25% of the time.

Physical Organization

The Count Chain is divided among three PC Boards: A101, A102, and A103, as follows:

Board A103 contains the first quinary unit, the following four DCUs, quad latches to load the information in the DCUs, and a multiplexer to place the information in proper time sequence for the front panel display. A variable +5 VDC supply for display brightness is also provided.

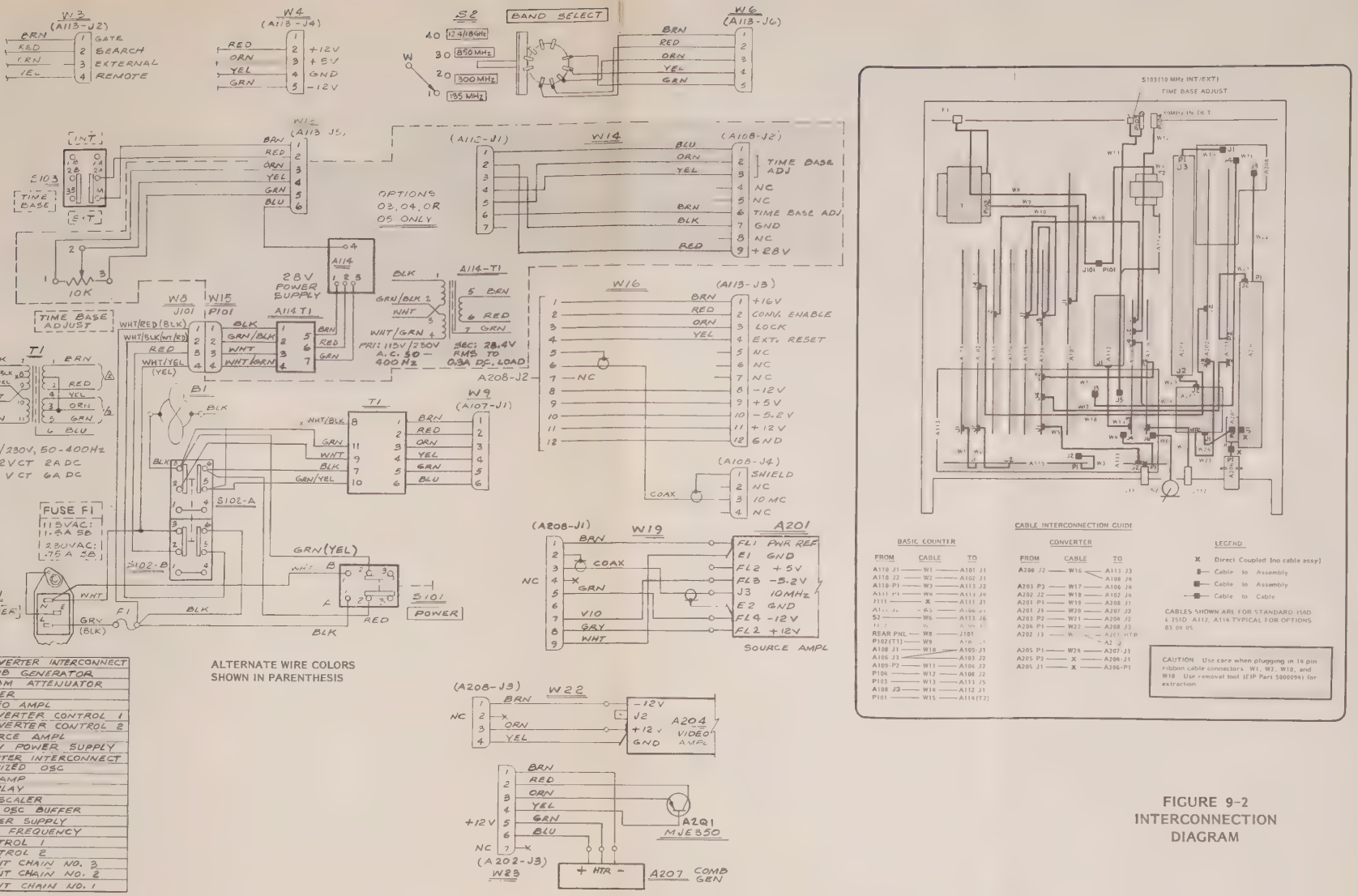
Board A102 includes the six remaining DCU's of the counting chain, a set of associated quad latches, and two multiplexers. Two decoders convert the multiplexer outputs to the seven line code which drives the visual display.

Board A101 includes the third decoder-driver, buffer circuits for the front panel **RESOLUTION** switches, timing circuits for the multiplexer and display. A101 also contains circuitry which suppresses zeros to the left of the first significant digit.

	LATCH - DISPLAY DIGIT POSITION										
	1	2	3	4	5	6	7	8	9	10	11
GATE TIME	10 GHz	1 GHz	100 MHz	10 MHz	1 MHz	100 kHz	10 kHz	1 kHz	100 Hz	10 Hz	1 Hz
1 sec.	1	2	3	4	5	6	7	8	9	10	11
100 ms.	1	2	3	4	5	6	7	8	10	11	
10 ms.	1	2	3	4	5	6	7	10	11		
1 ms	1	2	3	4	5	6	10	11	-		-
	NUMBER OF DCU SUPPLYING DATA TO LATCH										

TABLE 9-3A
DISPLAY DIGIT POSITION vs. SUPPLYING DCU

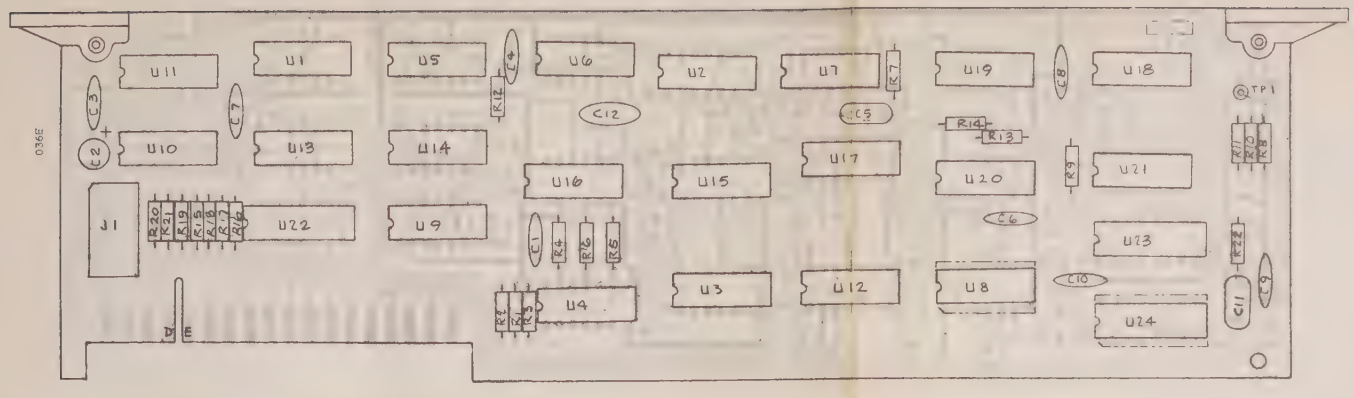
FIGURE 9-3A
COMPONENT LOCATOR
COUNT CHAIN 1 (A101)



A208	CONVERTER INTERCONNECT
A207	COMB GENERATOR
A206	3 dBm ATTENUATOR
A205	MIXER
A204	VIDEO AMPL
A203	CONVERTER CONTROL 1
A202	CONVERTER CONTROL 2
A201	SOURCE AMPL
A114	+28V POWER SUPPLY
A113	COUNTER INTERCONNECT
A112	OVENIZED OSC
A111	PREAMP
A110	DISPLAY
A109	PRESCALER
A108	REF OSC BUFFER
A107	POWER SUPPLY
A106	HIGH FREQUENCY
A105	CONTROL 1
A104	CONTROL 2
A103	COUNT CHAIN NO. 3
A102	COUNT CHAIN NO. 2
A101	COUNT CHAIN NO. 1

ALTERNATE WIRE COLORS SHOWN IN PARENTHESIS

FIGURE 9-2
INTERCONNECTION DIAGRAM



GATE TIME	5 COUNT	B	C	D
1 sec	5	0	0	0
100 ms.	4	0	0	1
10 ms	3	1	1	0
1 ms.	2	0	1	0
	1	1	0	0
	0	0	0	0

TABLE 9-3B
U15 PRESETS

COUNT CHAIN 1, 2, AND 3

Count Chain Boards 1, 2, and 3 (A101, A102, and A103) perform most of the actual frequency counting functions of the direct counter. The main components are: (1) a counting chain, (2) a storage unit, and (3) the display multiplexer.

The counting chain consists of a string of ten cascaded decimal counting units (DCUs), preceded by a quinary (÷5) counting unit. The quinary counter is sufficiently fast to follow the output of the binary (÷2) counter in the High Frequency Board, forming the first DCU. The remaining DCUs are each a standard integrated circuit having four output lines to indicate the state of the counter at any given time.

The storage unit is a string of quad latches, one for each of the eleven DCUs of the counting chain. An enable signal to the storage unit causes it to load the information from the DCUs.

The display multiplexer processes the information held in the eleven elements of the storage unit. The output of the storage unit is converted to the seven line code needed to drive the seven segments of each display digit. Power is applied to each digit sequentially for 25% of the time.

Physical Organization

The Count Chain is divided among three PC Boards: A101, A102, and A103, as follows:

Board A103 contains the first quinary unit, the following four DCUs, quad latches to load the information in the DCUs, and a multiplexer to place the information in proper time sequence for the front panel display. A variable +5 VDC supply for display brightness is also provided.

Board A102 includes the six remaining DCU's of the counting chain, a set of associated quad latches, and two multiplexers. Two decoders convert the multiplexer outputs to the seven line code which drives the visual display.

Board A101 includes the third decoder-driver, buffer circuits for the front panel RESOLUTION switches, timing circuits for the multiplexer and display. A101 also contains circuitry which suppresses zeros to the left of the first significant digit.

	LATCH - DISPLAY DIGIT POSITION										
	1	2	3	4	5	6	7	8	9	10	11
GATE TIME	10 GHz	1 GHz	100 MHz	10 MHz	1 MHz	100 kHz	10 kHz	1 kHz	100 Hz	10 Hz	1 Hz
1 sec	1	2	3	4	5	6	7	8	9	10	11
100 ms	1	2	3	4	5	6	7	8	10	11	
10 ms	1	2	3	4	5	6	7	10	11	-	
1 ms	1	2	3	4	5	6	10	11	-		
	NUMBER OF DCU SUPPLYING DATA TO LATCH										

TABLE 9-3A
DISPLAY DIGIT POSITION vs. SUPPLYING DCU

FIGURE 9-3A
COMPONENT LOCATOR
COUNT CHAIN 1 (A101)

COUNT CHAIN 1 (A101)

Count Chain 1 (A101) generates the correct timing sequence and control commands for the multiplex system, provides leading zero blanking of the display, and controls shifting of data from DCU to DCU in the counting chain in response to changes in gate time length.

In addition, A101 accepts the inputs from the front panel RESOLUTION switches, and processes them into control signals for the multiplex system and the Time Base Generator on Control 1 (A105). A101 also contains the third decoder driver for the display.

Multiplex System Operation

The multiplex system is composed of three individual multiplex channels designated MUX 1, MUX 2, and MUX 3. Each MUX channel includes a four-to-seven line decoder-driver which drives directly segments of the front panel display. MUX 1 controls the four most-significant digits of the display (10 GHz, 1 GHz, 100 MHz and 10 MHz). MUX 2 controls the middle three digits and MUX 3 the four least-significant digits. The input information for MUX 1, 2, and 3 is obtained from the eleven quad-latch units on Count Chains 2 and 3 (A102 and A103).

In order for each multiplex circuit and decoder to drive four digits, the multiplex timing sequence is broken down into four intervals designated Time Frames 1 through 4 (TF1 - TF4). Only one display digit in each channel is illuminated in a given Time Frame, as determined by the display digit selectors. The actual number displayed by the selected digit is determined by segment drive from the decoder-driver which drives all corresponding segments in that channel in parallel. If one of the selected digits is not to be illuminated, its segment drive is canceled by a blanking signal to the appropriate decoder-driver. Table 9-3C shows, for each channel and for each of the gate times, the relationship of the Time Frames to MUX address, the DCU addressed, the display digit selected by the MUX, and whether the drive is enabled.

For each available gate time, Table 9-3A shows the resulting position in the display at which the information from each DCU is presented. The DCUs not displayed in shorter gate times are those removed from the counting chain, as described in the paragraphs on Count Chain 3 (A103).

In addition to blanking digits 9, 10, and 11 of the display (as shown in Table 9-3A), three more digits may be blanked by depressing the appropriate RESOLUTION switches. The gate time remains at 1 ms. in these positions.

The MUX timing sequence is actually three groups of four time frames. The first two groups occur at a rate of 2.5 MHz, the last at 25 kHz. The fast groups are used only to gather zero suppression information; display occurs only during the slow group.

Multiplex Sequence Generator

Clock pulses for the multiplexer are obtained from a 2.5 MHz clock signal derived from the 10 MHz Time Base Oscillator (A116 or A112). This signal is processed through a circuit composed of DCUs U1 and U5, ÷16 U2, the inverters of U6, and the gates of U11. The "SET 9" inputs of the DCUs are tied together, so that applying a high level to this input causes the 2.5 MHz clock to be fed through the gates to U2 at a 2.5 MHz rate.

With a low "SET 9" the input to U2 is one-hundredth the 2.5 MHz rate, or 25 kHz. The "SET 9" inputs to U1 and U5 are the inverted D output from U2, which is high when U2 is reset. The clock to U2 is then at a 2.5 MHz rate for eight pulses after reset. The D output then switches, and the clock rate drops to 25 kHz for the next four pulses. The A and B outputs of U2, plus their complements, are combined in the four NOR gates of U7 to produce the four MUX timing signals TF1, TF2, TF3, and TF4. The output TF4 is combined with U2 output D, and applied to the J input of flip-flop U23B. The clock to U23 and U24 is the same as the input to U2. The end of the fourth slow clock pulse then triggers U23B which resets U2. The clock pulses then return to the 2.5 MHz rate. The next pulse resets U23B and returns U1, U2, and U5 to their initial states.

The result is to produce a frame consisting of eight MUX time intervals at the 2.5 MHz rate, followed by four at the 25 kHz rate. One extra clock pulse resets the generator. The drive to the front panel display from U10 is gated off by the D output of U2 during the eight fast pulses in this train.

Count Chain Data Shift Controls

As the length of the Gate Time is varied by changing the front panel RESOLUTION switches, the counting chain on A103 is also modified by removing DCUs from the string. This is described in the Circuit Description of Count Chain 3 (A103). In the 1 Hz RESOLUTION setting (1 sec. Gate Time), all eleven DCUs are in the counting chain. With 10 Hz RESOLUTION (100 ms. Gate Time), the seventh (10 kHz position) DCU is bypassed. With 100 Hz RESOLUTION the seventh and eighth DCUs are bypassed, and with 1 kHz RESOLUTION the seventh through ninth DCUs are bypassed.

As indicated in Table 9-3A, with shorter gate times, the information in the eighth through eleventh DCUs must be shifted into lower numbered latches (7 through 10) to read out and be displayed in the proper front panel position. The data shift controls which accomplish this function are produced in ICs U9, U13, U14, U15, and U16.

To allow the data shift to take place on A103, presettable DCUs are used in the counting chain. The output lines of the eleventh DCU feed the data input lines of the tenth DCU. The tenth DCU feeds data to the ninth DCU, the ninth feeds data to the eight, and the eighth feeds data to the seventh. When a LOAD DATA command is applied to one of these DCUs, it then loads data from and assumes the same state as the higher numbered DCU to its right. To shift data one place left in the highest five DCUs of the counting chain (DCUs 7 through 11), it is necessary to apply the data LOAD pulses in sequence to DCUs 7, 8, 9, 10, and then a reset pulse to DCU 11 (load zero), If the load pulses were applied simultaneously to all DCUs, they

would all go immediately to zero. The necessary sequence of pulses is produced by a 4-10 line decoder on A103 which is driven by a DCU on A101. The DCU is stepped through states 0 to 9 by a clock input, with the 1, 3, 5, 7, and 9 outputs of the decoder activating the load inputs of DCUs 7, 8, 9, 10, and 11 respectively. Every ten inputs to the data shift DCU on A101 cause the data in the DCUs on A103 to shift left one position.

To place the counting chain data in the proper position after the end of each gate time interval, clock pulses must be applied to the data shift DCU. With 1 second gate time, no pulses are required; with 100 ms. gate time, ten pulses are required; with 10 ms. gate time, 20 pulses; and with 1 ms. gate time, 30 pulses. The number of clock pulses is regulated by presettable DCU U15 and associated gates in U13, U14, and U16.

The ÷5 part of U15 is preset during the gate time to the states shown in Table 9-3B. Data inputs to produce them are the four gate control lines. The ÷2 part of U15 directly controls the gate through which the 2.5 MHz clock is applied to data shift DCU U9. With 1 second gate time, the binary is not preset, and no data shift clock pulses occur. With shorter gate time settings, the ÷2 is set during gate time, with data shift clock pulses occuring after gate time is complete. Every ninth pulse to the data shift DCU (U9) produces an output through AND gate U13 which is applied to the ÷5 input of U15. The input to U15 is combined with the D output in another AND gate, and applied to the ÷2 input. When the ÷5 count reaches zero state, the ÷2 state is also zero, and the data shift clock turns off. Depending upon the ÷5 preset state, either 0, 10, 20, or 30 clock pulses have occured, and the counting chain data has shifted 0, 1, 2, or 3 places to the left.

Additional gates inhibit the Sequence Generator during data shift. Update Data is also inhibited during this time.

Display Selector Drive Generator

This drive is actually the same as the MUX Time Frame signals during the slow scan. The signals TF1 - TF4 provide one input to each of the four NAND gates of U10. The other four inputs are tied together with the D output of U2. This D output is high only after the first eight fast scan signals (first two groups of TF1 - TF4) have occurred, and the slow scan (third group of TF1-TF4) is taking place. The NAND gate outputs are the inputs to the digit selector drivers on Display Board (A110).

Signal Generators for Blanking and Gate Time Controls

These generators operate on the inputs from the six front panel **RESOLUTION** switches. They are processed in the inverters of U4 and U8, and the NOR gates of U3 and U12, to produce nine output control signals. Five of these are used on A101 principally to control display blanking. The remaining four are used externally, as well as on A101. The four lines, one of which is high for each gate time, are fed to the gate generator on A105, which then determines the gate time. The signals are also fed to Count Chain 3 (A103) where they control the length of the counting chain as the gate time is changed. One of these four signals, plus the remaining five, are used on A101 to control least significant digit blanking by the **RESOLUTION** switches. Three outputs of U20 produce blanking signals in Display Driver 2, by combining MUX timing outputs TF2, TF3, and TF4 with the **RESOLUTION** switch signals from U4 and U8. This produces blanking in readout digit 7 (as indicated in Table 9-3C), plus blanking of digits 5 and 6 in resolution settings for 100 kHz and 1 MHz. U17 produces the blanking signals in Display Drive 3 (as indicated in Table 9-3C), plus complete blanking (TF1 - TF4) in the 100 kHz and 1 MHz resolution settings.

Leading Zero Suppression Circuitry

The portion of A101 related to leading zero suppression is detailed in Figure 9-3C. This function is accomplished in two steps. Initially, the circuit determines if any of the three channels contains non-zero data. If all data is zero, it disables the blanking and displays all zeros. If there is non-zero data, it locates the first channel containing this data.

The most vital portion of the zero suppression circuitry is contained within the decoder-drivers themselves. This is a zero detection circuit which is enabled by the ripple blanking input (RBI). If RBI is enabled (low), the presence of zero data causes the ripple blanking output (RBO) to be energized (low). The decoder-driver also contains a blanking input (BI) which blanks the digit when energized (low). BI and RBO are internally tied together so that the pin designated BI/RBO serves both as an input and an output. Thus, if RBI is enabled, zero data will energize RBO, which is equivalent to energizing BI, and the digit is blanked. Thus, a digit may be blanked either by applying a low-level to BI/RBO, or by the presence of zero data when RBI is enabled.

The first circuit function is to determine if any of the three channels contain non-zero data. All flip-flops are reset enabling the RBI on all decoder-drivers. As the multiplex system rapidly scans through its first four Time Frames, any non-zero data in a decoder-driver will be indicated by the RBO going high. This in turn enables the J input of the corresponding flip-flop. The next timing pulse sets that flip-flop and disables the RBI of that decoder-driver. At the end of the first multiplex group, the presence of any non-zero data is indicated by a set flip-flop. A set flip-flop enables the J input of the following flip-flop. This insures that non-zero data in any decoder-driver causes all flip-flops further down the chain to be set within two additional Time Frames.

If all data is zero, then the gating is such as to allow the eight clock pulse (TF4 of the second fast group) to set the first two flip-flops and enable the third. The ninth clock pulse then sets the third flip-flop. This then disables all ripple blanking inputs so no blanking will occur with all zero data.

The remaining task is to determine the first channel with non-zero data. Gates are arranged so that the ninth clock pulse will reset the first flip-flop which is in the "set" state via the K input, and thus enable the corresponding RBI, prior to the start of the slow scan. The internal ripple blanking circuitry will then blank all zeros until the first non-zero data is present.

Gate Time	Sequence Time Frame in MUX Sequence	MUX Address a	MUX Address b	CHANNEL 1 DCU Addressed	CHANNEL 1 Display Digit Selected	CHANNEL 1 Drive Enable	CHANNEL 2 DCU Addressed	CHANNEL 2 Display Digit Selected	CHANNEL 2 Drive Enable	CHANNEL 3 DCU Addressed	CHANNEL 3 Display Digit Selected	CHANNEL 3 Drive Enable
1 sec.	TF-1	0	0	1	1	+	5	5	+	8	8	+
	TF-2	1	0	2	2	+	6	6	+	9	9	+
	TF-3	0	1	3	3	+	7	7	+	10	10	+
	TF-4	1	1	4	4	+	11	7	-	11	11	+
100 ms.	TF-1	0	0	1	1	+	5	5	+	9	8	+
	TF-2	1	0	2	2	+	6	6	+	10	9	+
	TF-3	0	1	3	3	+	7	7	-	11	10	+
	TF-4	1	1	4	4	+	8	7	+	8	11	-
10 ms.	TF-1	0	0	1	1	+	5	5	+	10	8	+
	TF-2	1	0	2	2	+	6	6	+	11	9	+
	TF-3	0	1	3	3	+	7	7	-	8	10	-
	TF-4	1	1	4	4	+	9	7	+	9	11	-
1 ms.	TF-1	0	0	1	1	+	5	5	+	11	8	+
	TF-2	1	0	2	2	+	6	6	+	8	9	-
	TF-3	0	1	3	3	+	7	7	-	9	10	-
	TF-4	1	1	4	4	+	10	7	+	10	11	-

TABLE 9-3C
GATE TIME vs. SEQUENCE TIME FRAME and DCU ADDRESSED

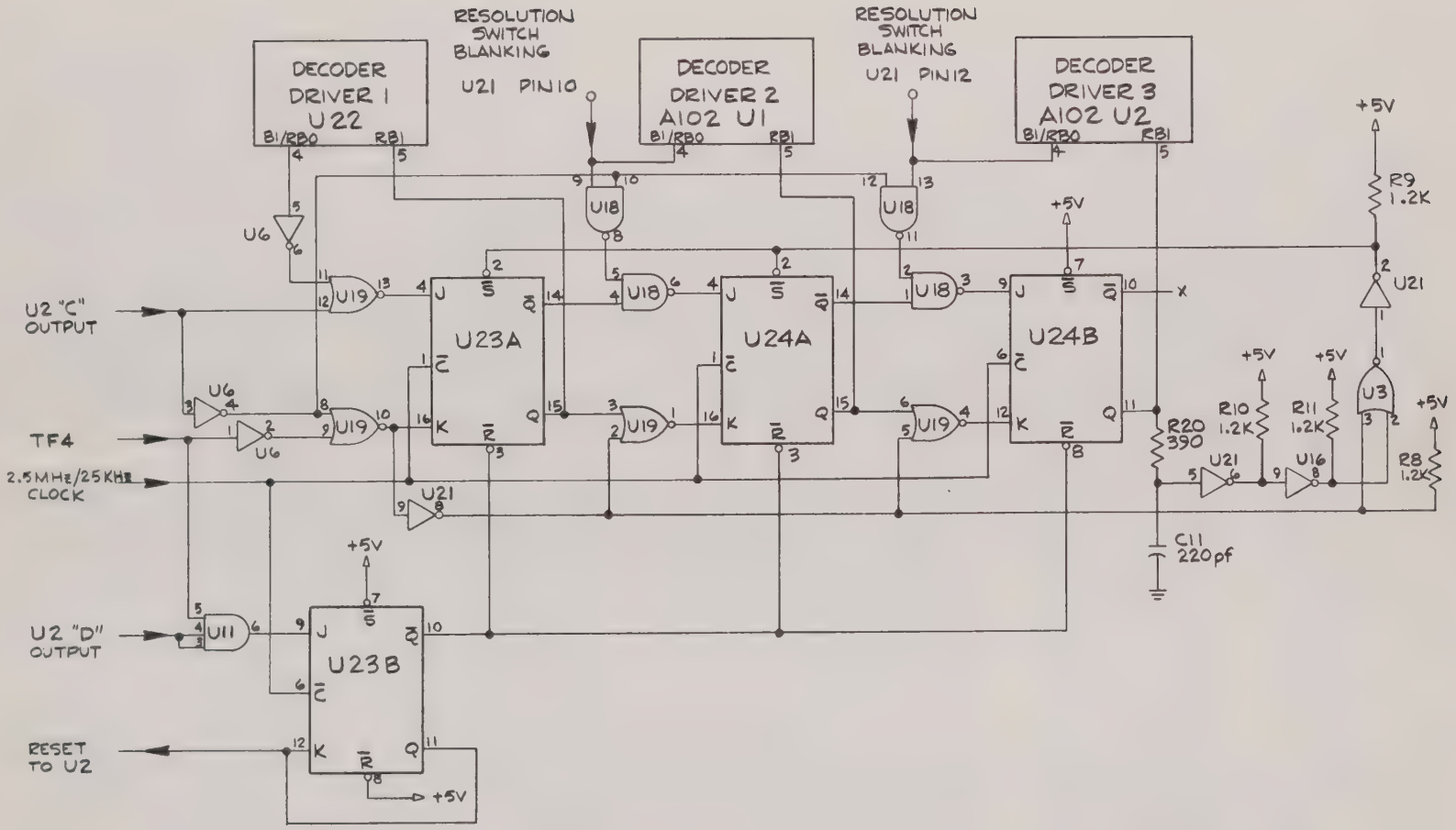
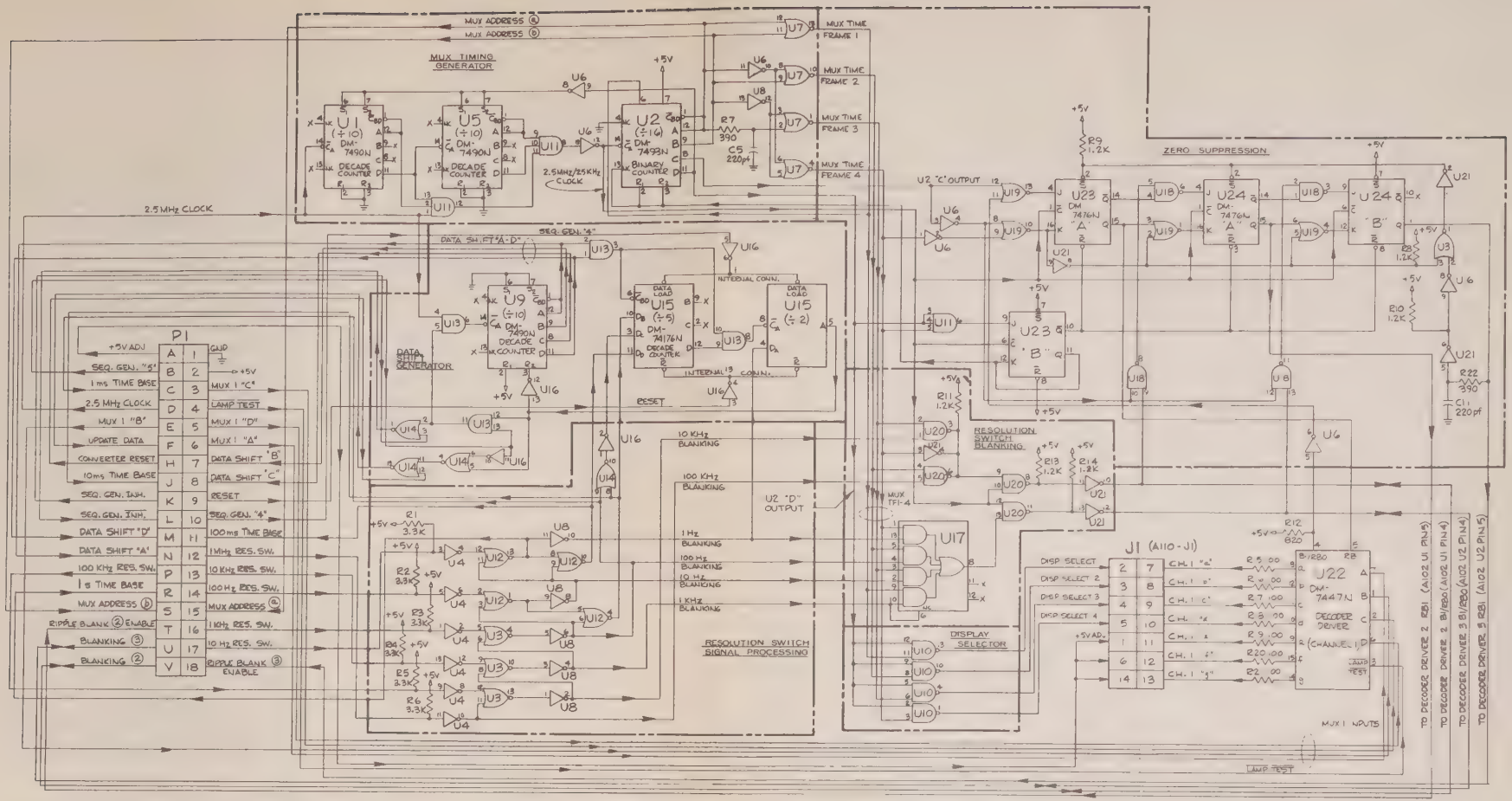
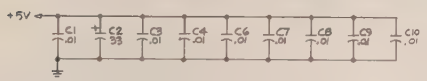


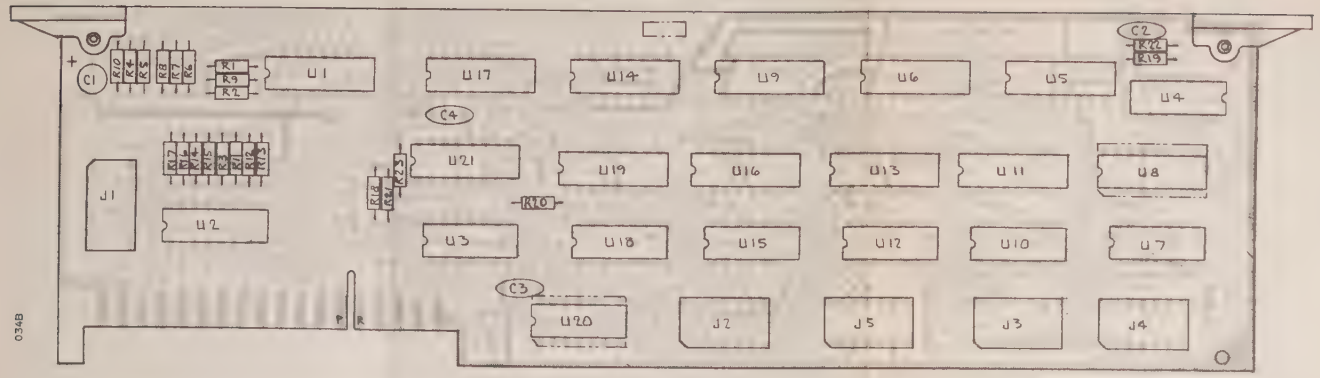
FIGURE 9-3C
PARTIAL SCHEMATIC
LEADING ZERO SUPPRESSION





I.C. NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1, U5, U9	DM7490N	10	5
U2	DM7493N	10	5
U3, U7, U12, U14, U19	DM7402N	7	14
U4, U6, U8, U16	DM7404N	7	14
U10	DM7401N	7	14
U11	DM7411N	7	14
U13	DM7408N	7	14
U15	DM7476N	7	14
U17	DM7454N	7	14
U18, U20	DM7400N	7	14
U21	DM7405N	7	14
U22	DM7447N	8	16
U23, U24	DM7476N	13	5

FIGURE 9-3B
SCHEMATIC DIAGRAM
COUNT CHAIN 1 (A101)

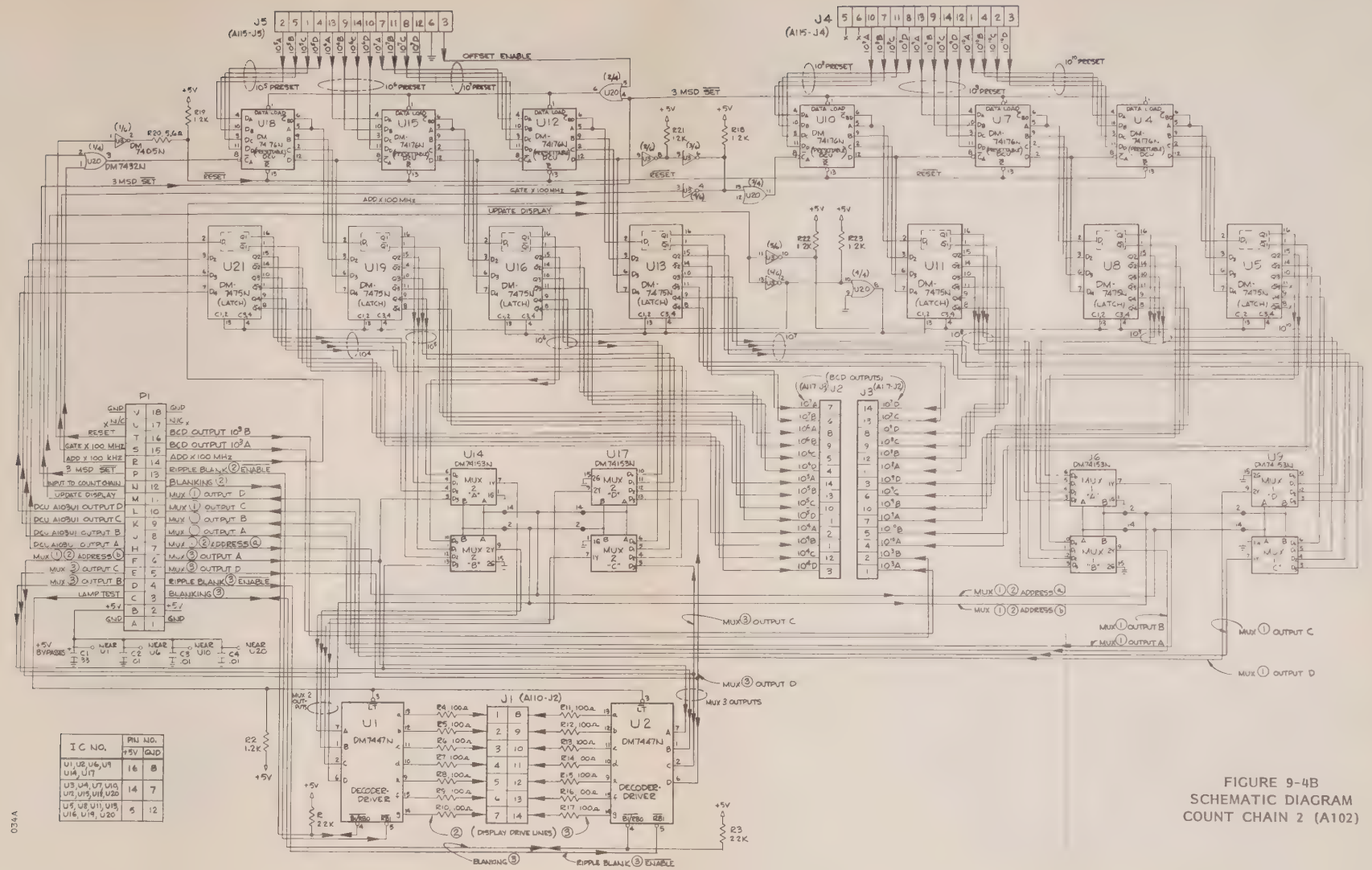


COUNT CHAIN 2 (A102)

A102 is similar to A103, being simply a continuation of the counting chain that begins on A103. Six DCUs on A102 (U4, U7, U10, U12, U15, and U18) combine with the five DCUs on A103 for a total of eleven in the counter. Each of these six are presettable. They are programmed by data lines either from the Converter (when it is being used), or from external inputs when IF Offset Option 06 is used.

Each of the six DCUs has an associated quad-latch (U5, U8, U11, U13, U16, and U19) to store the DCU information. An additional latch (U21) stores the information from the last DCU on A103 (U1), which does not have a quad-latch on that board. Two sets of multiplexers (U6 and U9, and U14 and U17) transfer the information from the latches to the display drivers. Two decoder-drivers (U1 and U2) convert the four line BCD information from the two multiplexers into the seven-line code necessary to drive the segments of the front panel display. Separate inputs to these decoders allow the display to be blanked, or to display all eights in the Visual Display Test. (A more detailed description will be found in the paragraphs titled "Leading Zero Suppression Circuity".)

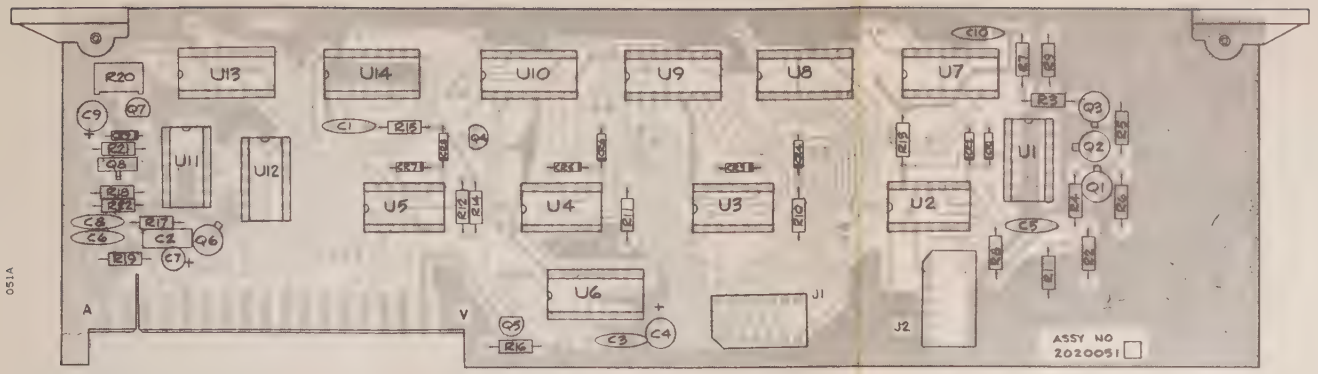
FIGURE 9-4A
COMPONENT LOCATOR
COUNT CHAIN 2 (A102)



IC NO.	PIN NO. +5V	PIN NO. GND
U1, U2, U6, U9 U14, U17	16	8
U3, U4, U7, U10, U12, U15, U18, U20	14	7
U5, U8, U11, U13, U16, U19, U20	5	12

034A

FIGURE 9-4B
SCHEMATIC DIAGRAM
COUNT CHAIN 2 (A102)



COUNT CHAIN 3 (A103)

A103 receives BCD and carry signals from the High Frequency Board (A106). The carry signal is processed thru one to four decade dividers (U2-U5), with the carry output at P1 pin E sent to the Count Chain 2 Board (A102). Gate width commands from the RESOLUTION switches, control data routing and shifting to place the data in proper position for display. Display data for 1 Hz thru 1 kHz information is stored on this board, with mux commands from the Count Chain 1 Board (A101) controlling the transfer of this data to the front panel display.

Data from the first DCU on A106 enters at J2. The data consists of four TTL logic bits giving the BCD information from the first decade, and a 60% duty cycle ECL logic signal which is the carry output from the first decade.

The ECL carry signal enters the ECL-to-TTL converter on the base of Q1. R1 and R2 provide a 95 ohm termination to -1.4 V (open circuit voltage at J2 pin 3). R5 and R6 provide a reference voltage of -1.5 V at the base of Q2. Q1, Q2, and Q3, form a differential cascode amplifier operating in the over-driven mode as a level translator. R3 prevents the TTL output signal from going negative.

The TTL carry signal enters a cascade of four DCU's (U2-U5). The carry output from A103 can be selected from any one of the four DCU's by a 4-wide, 2-input AND-OR-INVERT gate (U12). The selection of the carry output is determined by the RESOLUTION switches. For 1 second gate times, the output comes from U5; for a 0.1 sec gate time, from U4, etc.

There are four latches on A103 (U7-U10) which contain the information to be displayed by the 1 Hz thru 1 kHz digits. The input to these latches comes from the first four decade dividers: input to U7 comes from the decade divider on the High Frequency Board (A106), input to U8 from A103U2, to U9 from A103U3, and to U10 from A103U4.

When the counter is operated in shorter gate time than one second, the decade dividers contain correspondingly higher digit information. For example: For a 0.1 second gate, the first DCU (on A106) contains the 10 Hz information; for a .01 second gate, 100 Hz information, and for a 1 ms gate, 1 kHz information. In order for this information to be displayed properly, BCD information in the DCU's is shifted to the right before it is transferred to the storage latches. The data shift occurs in sequence from right to left; that is, the data moves from U4 to U5, then from U3 to U4, from U2 to U3, and finally from J2 to U2. This shift sequence is controlled by the four command signals: Data Shift A thru Data Shift D, generated on A101. This series occurs once for 10 Hz resolution (100 ms gate), twice for 100 Hz resolution (10 ms gate), and three times for 1 kHz resolution and above (1 ms gate). During the data shift process, the normal clock inputs to the DCU's must be inhibited. This is accomplished by one third of U11, and the four diode gates (CR1, CR4, CR6, and CR8). These gates are held off during sequence 5 when the data is being shifted.

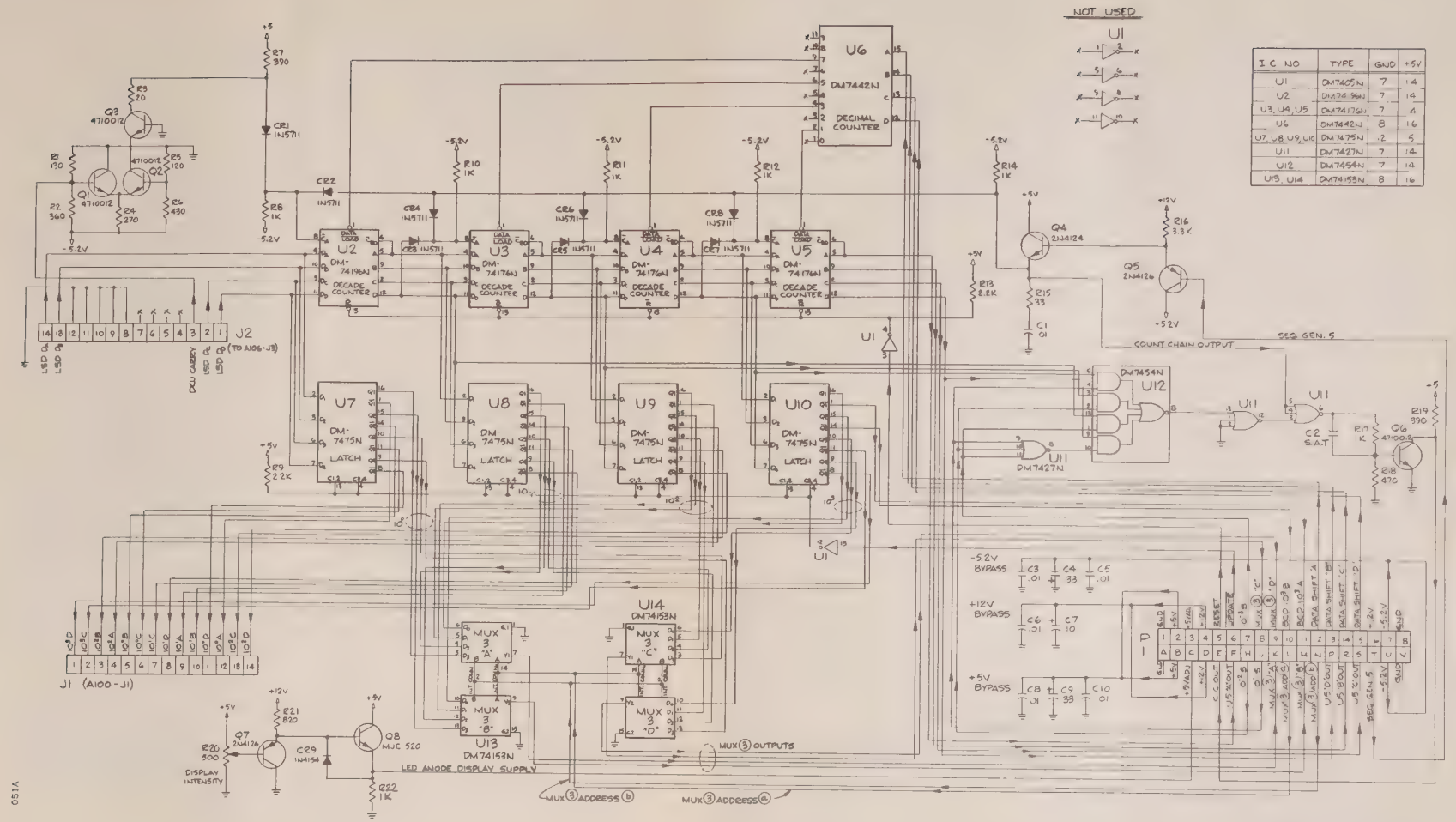
Reset of the four DCU's is controlled by the counter reset line, and occurs after the data is read into the latches and before the next counter gate period. The inverted BCD information from the latches goes to J1 for use with the BCD Output option.

The non-inverted BCD data from the four latches goes to a 4-by-4 mux consisting of U13 and U14. This data is then sent four bits at a time, to the Count Chain 2 Board (A102), where it is converted into 7-segment display information to drive the front panel LED display. The control signals for the mux switch come from A101 and are comprised of two signals: mux address a, and mux address b. These two signals form a binary code to give four addresses: 0, 1, 2, and 3, as shown in Table 9-5A.

SELECTED INPUT	ADDRESS	
	A	B
0	0	0
1	1	0
2	0	1
3	1	1

TABLE 9-5A
MULTIPLEX ADDRESS

FIGURE 9-5A
COMPONENT LOCATOR
COUNT CHAIN 3 (A103)



I C NO	TYPE	GND	+5V
U1	DM7405N	7	14
U2	DM74196N	7	14
U3, U4, U5	DM74176N	7	4
U6	DM7442N	8	16
U7, U8, U9, U10	DM7475N	12	5
U11	DM7427N	7	14
U12	DM7454N	7	14
U13, U14	DM74153N	8	16

FIGURE 9-5B
SCHEMATIC DIAGRAM
COUNT CHAIN 3 (A103)

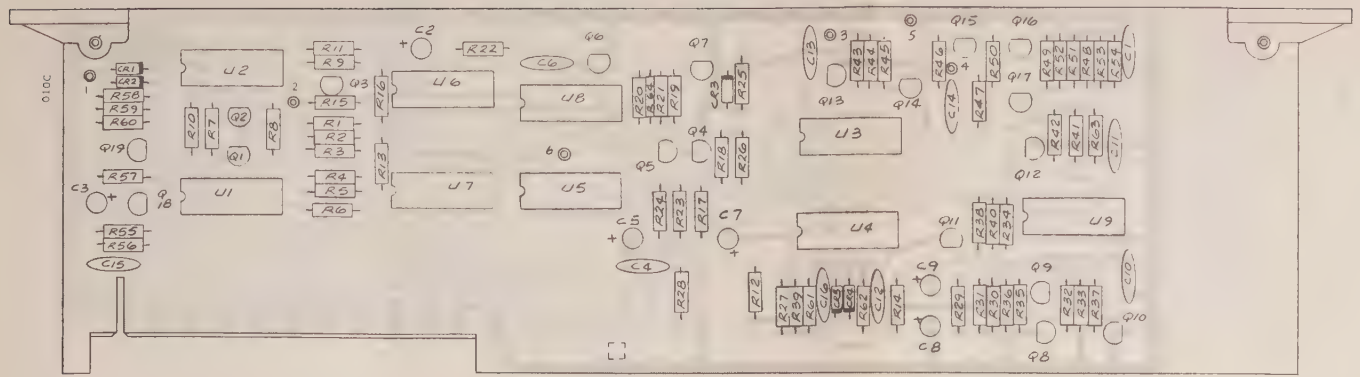


FIGURE 9-6A
COMPONENT LOCATOR
CONTROL 2 (A104)

CONTROL 2 (A104)

This unit accepts commands from the front panel controls, programming inputs and internal control inputs. Front panel controls include RESET, TEST, and BAND SELECT. Internal control inputs to this unit are: SEQUENCE GENERATOR "0", SEQUENCE GENERATOR "5", SEQUENCE GENERATOR "8", PRINT command, and Converter LOCK. The outputs of A104 consist of counter control signals and a front panel SEARCH indicator.

Circuit Description

The three Band Select input lines from P1 pins 6, 7 and 8, each drive an inverter in U1 when one particular line is grounded. The outputs drive the emitters of transistor switches Q1, Q2, and Q3. Their collectors connect directly to the Band Selection inputs on the High Frequency Board, and energize the appropriate input channel amplifier for that band. In Band III, however, the Q3 drive signal is combined with two other inputs via three inverters with open-collector outputs. The three inputs are: the BAND III SELECT (low in Band III), the LOCK signal (low when Converter is locked), and the TEST signal (low except in the TEST mode). The counter must then be in Band III, with the Converter locked and the unit not in the TEST mode for the Band III input to be enabled.

If all the BAND SELECT commands are disabled (as when switching bands), a RESET is generated. This is accomplished by combining the inputs to drive U5 pin 10. This OR gate then drives the RESET trigger U9 pin 5.

Manual Reset and Test inputs come from front panel RESET and TEST switches, and are fed through resistor-capacitor networks to Schmitt triggers composed of Q15, -16, -17, and Q8, -9, -10 respectively. These circuits are used to eliminate the effects of switch contact bounce.

The output of the TEST trigger generates the TEST command for A105, and the TEST signal. These signals are differentiated and fed to the base of Q11, which then triggers the RESET command at both start and finish of the TEST cycle. The TEST signal also drives the bases of Q1-Q3, disabling the input channels of A106 during the TEST cycle. The TEST signal also removes BAND II ENABLE, returning gate time to normal. Finally it combines with the Manual Reset to produce the Visual Display Test function of U7 pin 11.

The Manual Reset also drives the RESET trigger through C11 and Q12. This trigger drives the one shot U8 to produce the RESET pulse.

The CONVERTER RECYCLE command is generated at U7 pin 3, and is generated by either a Manual Reset, a band switching RESET, or after initial instrument turn on. At turn on, the circuit composed of Q4, Q5, and Q6 holds U8 in the triggered state for several seconds. This output sets the Sequence Generator on A105 to "9" and is equivalent to resetting the counter.

In Band III, a LOCK command is received from the Converter when a signal is acquired. This signal generates a Reset through Q14. It is also combined with the Band III SELECT command to drive the SEARCH indicator (U4 pin 8) on the front panel. In the event that the Converter loses LOCK, the one shot U6 is triggered. The output of U6 inhibits the Sequence Generator to allow the Converter to reacquire the signal without displaying zeros on the readout. If a LOCK command is not obtained within the one shot period, a RESET is generated via Q13. If a LOCK signal is reacquired, the delay time is reduced to a few milliseconds by Q18 and Q19.

In the event that the Sequence Generator is in the PRINT or memory update portion of the cycle when LOCK is lost, the sequence is allowed to continue to the Display period where it is held. This is accomplished by combining in an OR gate, the PRINT command and SEQUENCE GENERATOR "5", and then combining these with the output of U6 at U5 pin 11. When LOCK is reacquired, the counter is immediately reset.

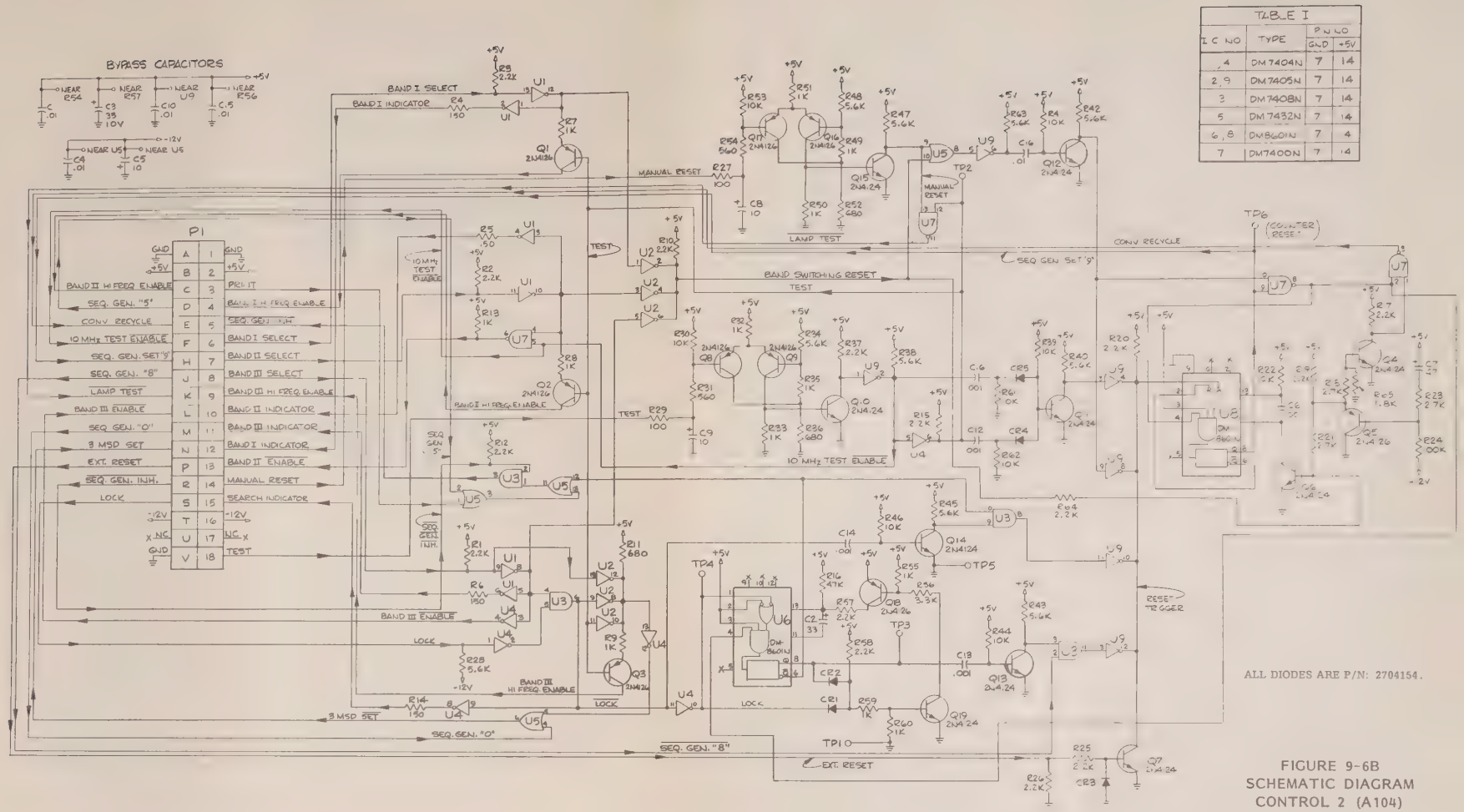
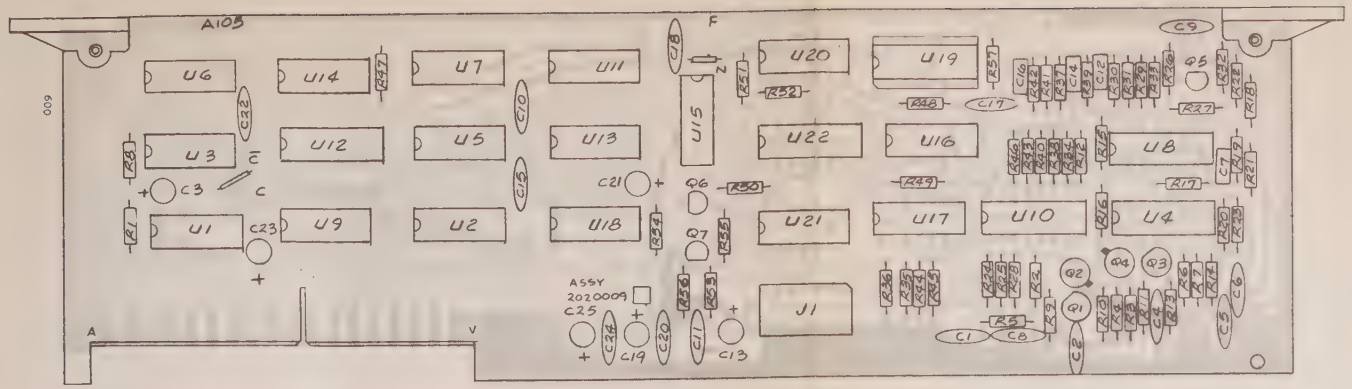


TABLE I			
I C NO	TYPE	P N NO	
		GND	+5V
1,4	DM7404N	7	14
2,9	DM7405N	7	14
3	DM7408N	7	14
5	DM7432N	7	14
6,8	DM8601N	7	4
7	DM7400N	7	14

ALL DIODES ARE P/N: 2704154.

FIGURE 9-6B
SCHEMATIC DIAGRAM
CONTROL 2 (A104)

010F



CONTROL 1 (A105)

This unit contains the circuitry to generate the counter control sequence and the gate time interval. These functions are derived from the 10 MHz Time Base Oscillator.

Clock Generator

Transistors Q1 through Q4 form a Schmitt Trigger to convert the 10 MHz time base signal to a square wave suitable to drive the ECL gates of U4. These outputs are further gated and translated to TTL levels in U8.

Sequence Generator

This circuit produces the main control cycle of the counter by generating a sequence of commands. It consists primarily of an address generator U9, and a decoder U12.

Clocking is performed at a 100 kHz rate by dividing the 10 MHz TTL clock in DCU's U2 and U7. An output of 2.5 MHz is also obtained at U7 pin 12 for the multiplexer clock on Count Chain 1 (A101). The gates of U5 are arranged so that both the 100 kHz and the 2.5 MHz signals are trains of 50 ns wide pulses.

The 100 kHz pulse train drives address generator U9, which produces a four line BCD code. The A and B outputs of U9 address U12, while the C output selects which of the two decoders is active. This generates sequential control signals, one on each of eight lines. Two more signals are obtained using the D output of U9 by itself, or combined with the A output. The gate inputs to U12 (pins 2 and 14) are turned off during switching and when not required, by an OR gate in U13. This eliminates any outputs due to switching transients.

Several internal counter operations inhibit the sequence generator. In addition, Digital Output Option 09, and Remote Programming Option 07, allow the sequence to be externally inhibited.

Gate Generator

The Gate Generator provides the correct gate time interval as required by the front panel **RESOLUTION** switch settings. The time interval is controlled by selecting an integral number of cycles of the 10 MHz Time Base Oscillator. This then turns the Gate Binary U10 on and off appropriately.

The major element of the Gate Generator is a programmable multi-decade divider, U19. By applying the proper address as shown in Table 9-7B, division ratios from 10^3 to 10^6 can be obtained. A 1 MHz input is then used to generate intervals from 1 ms to 1 second. DCU U16 divides the 10 MHz clock signal to provide the 1 MHz input for U19. The address is obtained by processing the four gate control signals from A101.

For operation in Band II, it is necessary to expand the gate time by a factor of four, since the incoming frequency is divided by four. This is accomplished by disabling Q5. The 2.5 MHz signal from U2 and U7 then appears at U8 pin 15 during the gate time and is combined with the 10 MHz signal to produce a 2.5 MHz pulse train at U17 pin 3. If Q5 is enabled, then the 10 MHz pulse train will appear there.

The Q_B output of U22 is combined in U17 with the 10 MHz clock and the A and D outputs of U16 to produce the Time Base Gate Level at U17 pin 6. This arrangement guarantees that the gate time interval is precisely determined by the 10 MHz signal itself.

It is necessary that the Q_B output be no more than one microsecond duration. The two flip-flops of U22 are interconnected in such a manner as to produce a single one microsecond pulse every time the output of U19 goes low.

Display Time Generator

This generator consists of U18, U15, Q6, Q7 and associated circuitry. Triggering the multivibrator U18 generates a pulse whose width is determined by C21 and the resistance of the front panel **SAMPLE RATE** potentiometer. Q6 is a current amplifier to increase the available range, while DCU U15 is used to scale the range by a factor of ten. The result is a display time period variable from approximately 60 ms to 40 seconds. U18 is triggered by the SEQUENCE GENERATOR "8" appearing at pin 2. Once turned on, feedback from Q7 to pin 4 holds the unit in its free running state until pin 3 goes low. Pin 3 input is derived from the output of DCU U15. The Display Time Generator output (U3 pin 12) is then used as one of the Sequence Generator Inhibit inputs.

The Display Time cycle begins with SEQUENCE GENERATOR "9" setting U15 (pin 7) to the "9" state which inhibits U18 (pin 3) from triggering. When SEQUENCE GENERATOR "7" begins, U15 is reset (pin 3), thus enabling U18. Period "8" triggers U18 (pin 2) and the Sequence Generator is then held in period "8" until U15 counts to 9, at which time the display period ends.

Application of the front panel HOLD command at U13 pin 8, holds U15 in the reset position so that the Sequence Generator is permanently inhibited in period 8.

To assist troubleshooting of the Sequence Generator, a Cycle Speed jumper is provided. If this jumper is moved from +5 (Normal) to ground (Fast), the R(1) input (U15 pin 2) is brought low, and the Display Generator is inhibited, thus reducing the display time to 10 microseconds.

CONTROL LINE			DIVISION RATIO
2^0	2^1	2^2	
1	1	0	10^3
0	0	1	10^4
1	0	1	10^5
0	1	1	10^6

TABLE 9-7B
PROGRAMMABLE DIVIDER

FIGURE 9-7A
COMPONENT LOCATOR
CONTROL 1 (A105)

PERIOD	FUNCTION	DURATION	LOCATION
9	COUNTER RESET	10 µs	-
0	3 MSD $\overline{\text{SET}}$	10 µs	U12 pin 9
1	OFFSET ENABLE	10 µs	U12 pin 10
2	GATE GENERATOR SET	10 µs	U12 pin 11
3	GATE GENERATOR ENABLE	10 µs	U12 pin 12
4	GATE PERIOD	GATE + 10 µs	U12 pin 7
5	$\overline{\text{DATA UPDATE}}$	10 µs	U3 pin 10
6/7	PRINT	20 µs	U14 pin 6
8	DISPLAY PERIOD	Variable	U9 pin 11

TABLE 9-7A

SEQUENCE GENERATOR COMMANDS

Commands are generated as shown in Table 9-7A. (Period numbering is determined by the output state of U9.) The sequence proceeds as follows:

Period 9: The starting point in the cycle. All counting chain DCU's are reset.

Period 0: In Band III, the YIG/Comb Generator frequency is preset.

Period 1: Used to preset counter in conjunction with Offset Option 06.

Period 2: The Gate Generator is set.

Period 3: The Latch Binary (U10B) is reset, enabling the Gate Binary (U10A). The 10 MHz clock (U8 pin 7) is applied to the Gate Generator.

Period 4: The Gate Generator is enabled and inhibits the Sequence Generator (U13 pin 8) for the duration of the gate time. The incoming signal to the counter is counted during this period.

Period 5: The accumulated data in the counting chain DCU's is loaded into the latches.

Period 6/7: The PRINT command is generated indicating the presence of data on units equipped with Digital Output Option 09.

Period 8: The Display Period. The Display Generator is turned on and inhibits the Sequence Generator during this time. The duration of the period is determined by the front panel SAMPLE RATE control.

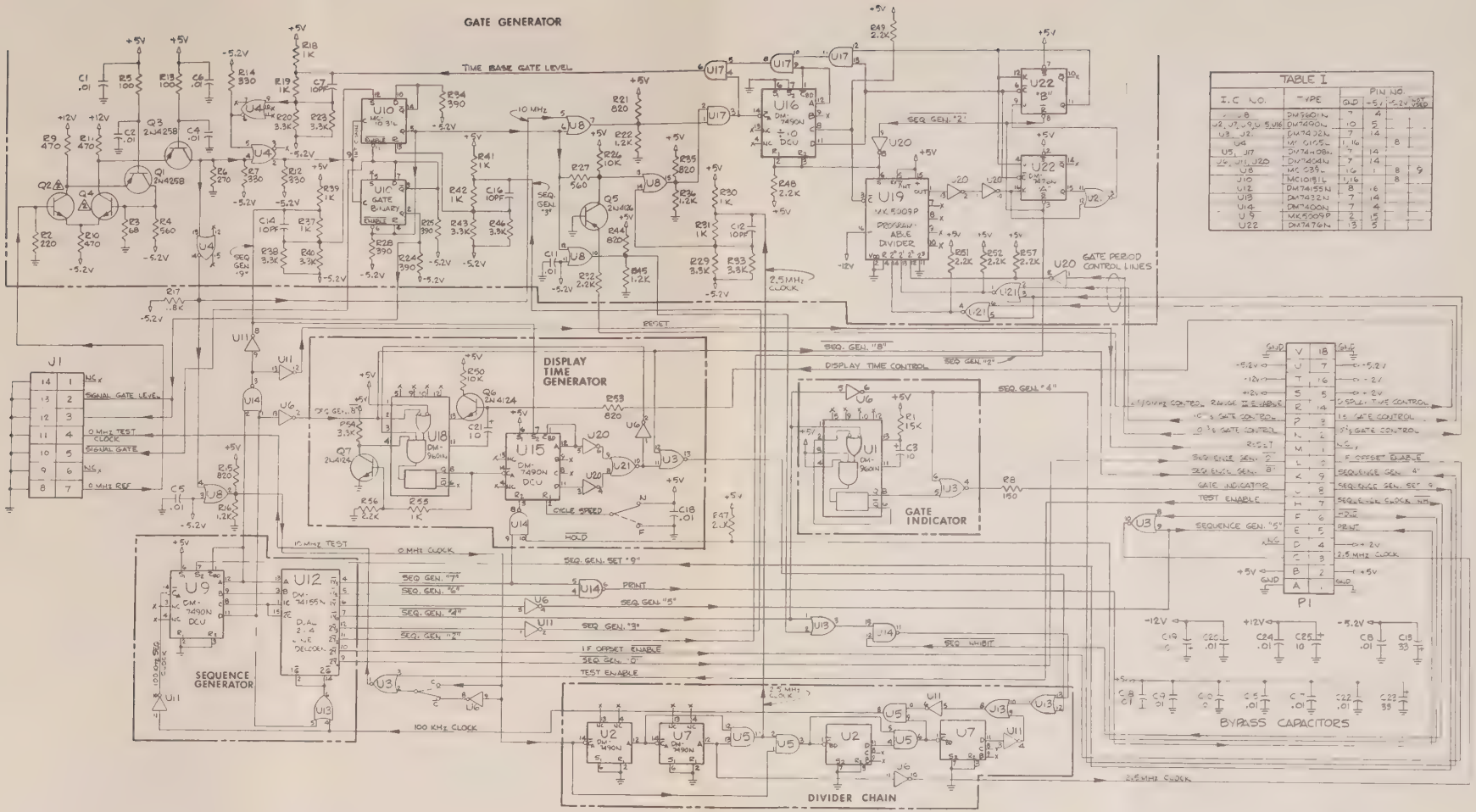
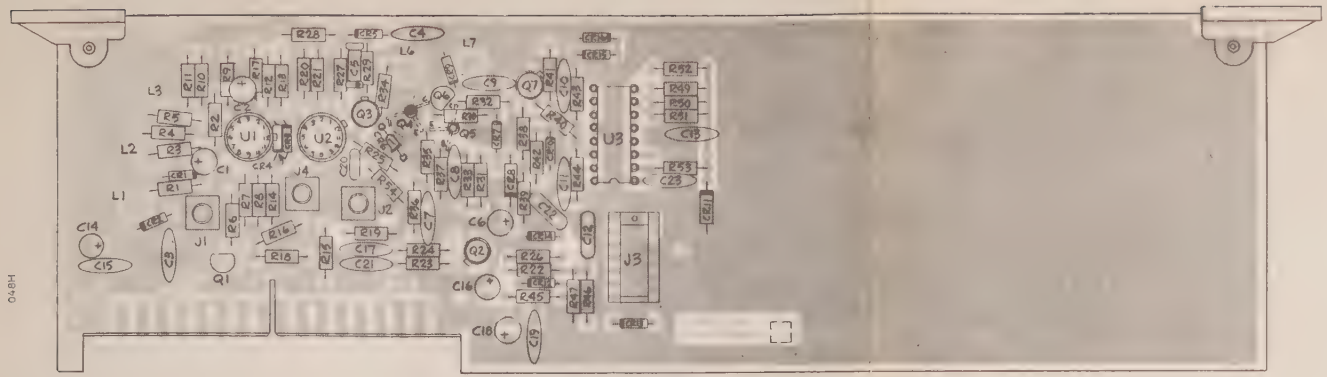


TABLE I

I.C. NO.	TYPE	PIN NO. GND	+5V	-5.2V	-12V
U1, U3, U4, U6, U8	DM7490N	7	4		
U2, U7, U9, U15, U16	DM7490N	10	5		
U13, U21	DM7400N	7	14		
U14	MC 1035	1, 16		8	
U5, U17	DM74H08N	7	14		
U6, U11, U20	DM7404N	7	14		
U18	MC 1035	16	1	8	9
U10	MC10181L	1, 16		8	
U12	DM74155N	8	16		
U19	DM7432N	7	14		
U14	DM7400N	7	4		
U9	MK5009P	2	15		
U22	DM7476N	13	5		

FIGURE 9-7B
SCHEMATIC DIAGRAM
CONTROL 1 (A105)



HIGH FREQUENCY (A106)

The High Frequency Board accepts RF signals from the Preamplifier (A111), Prescaler (A109), Converter (A2), and gate and 10 MHz Test signals from Control 1 (A105). Range signals from Control 2 (A104) select the appropriate input which is processed, gated, and counted in the first decade counting unit (DCU). The outputs from A106 are the carry (f/10) signal, and the first decade of BCD information. These signals go to Count Chain 3 (A103) for further processing.

A106 accepts three input signals on J1, J2, and J4, and a 10 MHz Test signal on J3 pin 4. One of the three inputs is selected by a command signal entering on pins 12, 13, or 14 of P1. Each command line sits at approximately -12 V until it is selected, at which time it is pulled up to about + 0.7 V. This command signal, thru the appropriate resistor divider, brings the base of a current source transistor up to about -6 V, turns on the appropriate differential amplifier, and allows a signal to pass thru. The signal entering each gated amplifier is terminated with a 51 ohm resistor and a small inductor in series with the resistor to compensate for transistor loading at high frequencies. The net combination keeps the input VSWR below 1.5:1 up to 400 MHz.

If the input to J1 is selected, an additional amplifier stage (U1A) is also turned on by the control signal. (Q1 is used to prevent excess loading of the control line.) The input impedance of this amplifier is matched in the same way as the J2 and J4 inputs, however there are two limiting diodes for the J1 input to prevent overdriving the first stage.

The signal is ac-coupled into the preamplifier stage to allow the input to be biased at approximately -6 V. The collectors of U1A are operated against ground to minimize parasitics. L2 and L3 in series with load resistors R3 and R5, are high frequency peaking coils used to flatten the response of the amplifier. R4 is used partly as a damping resistor for L2 and L3, and partly to establish a -2 V level at the output of U1A for direct coupling to U1B. CR3 and CR4 act to prevent large signals from overloading U1B.

The input selector differentially drives squaring circuit Q3 and CR6. Q3 is a current mirror which is used as a voltage-to-current converter. The current from Q3's collector is used to drive tunnel diode CR6. The action of a tunnel diode under a current driving signal is that of a Schmitt trigger; that is, the voltage across the diode changes abruptly between two states (<0.2 and 1 V). This characteristic converts the sine wave current into a square wave voltage signal, which can be used to drive the pulse forming network.

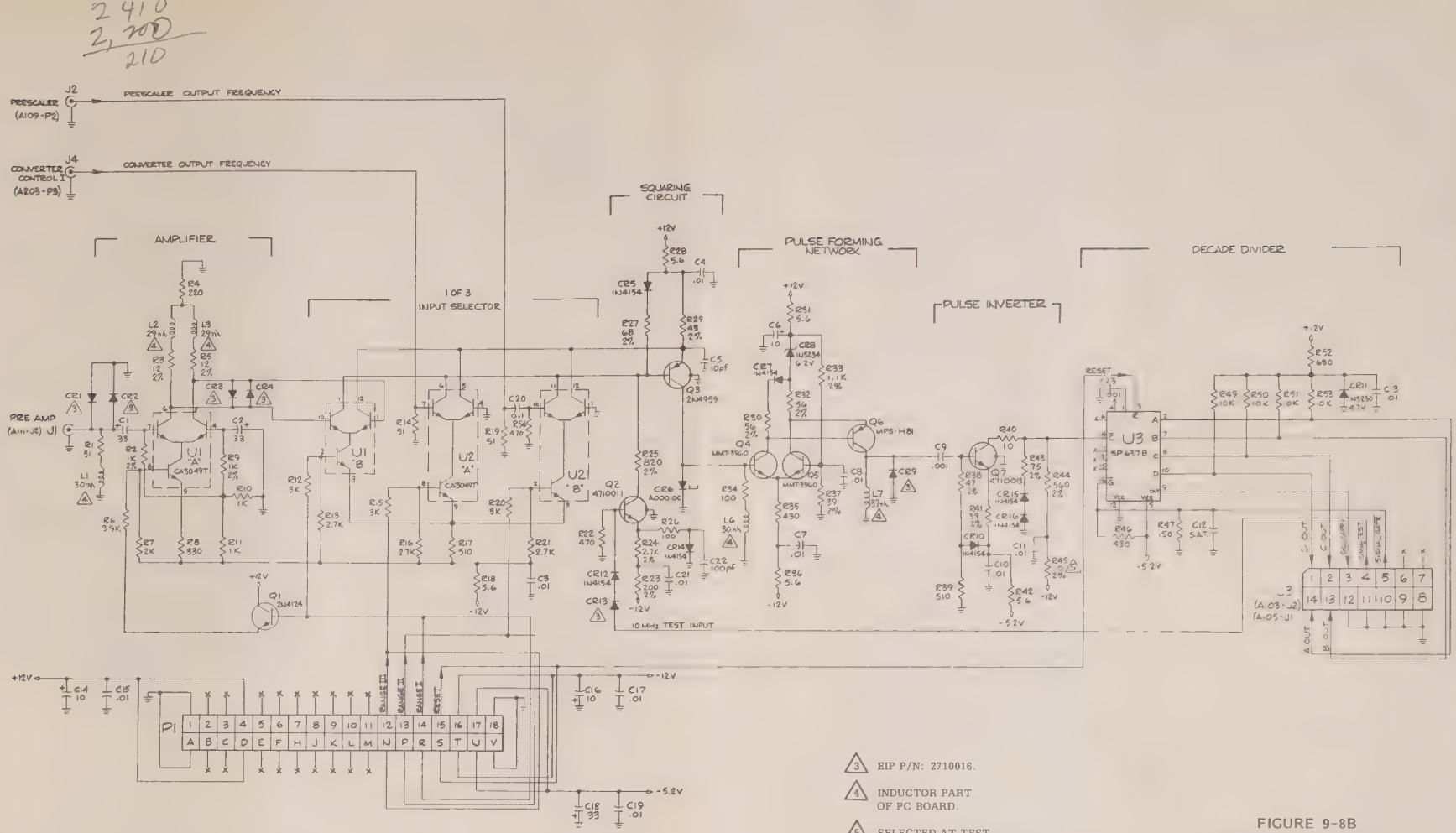
The pulse forming network input is a wide-band high speed differential amplifier (Q4/Q5), to increase the amplitude of the tunnel diode signal, and improve the rise and fall times. The output of Q4/Q5 drives current mirror Q6, used here as a current switch. Essentially, Q6 is either on or off, but the output is the current from the collector, and not a voltage signal. The switched current signal drives differentiator L7. The output of a differentiator with a square wave input is a series of pulses — positive when Q6 turns on, and negative when Q6 turns off. The negative pulses (wider than the positive pulses due to transistor storage time) are removed by CR9. Shorting out the negative pulses also provides a damping effect on L7, improving its response to the positive pulses at high frequencies.

These positive pulses are then coupled to pulse inverter Q7, which has two functions: to invert the pulse, and to deliver the negative output pulses at the right dc reference level for decade divider U3. A stable dc reference is provided by resistive divider R43, R44, and R45. The voltage from this divider is as stable over time and temperature as the -12 V power supply. The inverter is kept from disturbing this reference by being biased just at cutoff. This is accomplished by developing a forward bias for the transistor from the voltage drop across CR10, whose voltage matches the base-emitter voltage of Q7, keeping Q7 just at the edge of conduction. Basically, Q7 is a pulse amplifier, since it only conducts during a signal pulse. The load resistor for Q7 is the net equivalent of the bias network R43-R45.

Q7 output drives the input of decade divider U3. The divide-by-ten output of U3 is a 60/40% duty cycle ECL level signal, and is called the "DCU CARRY" signal (J3 pin 3); the load resistor for this signal is located on A103.

The gate signal to the DCU is an inverted ECL signal. It enters on J3 pin 5, and goes directly to U3 pin 16. The BCD output information is available at J3 pins 1, 2, 13, and 14. During a count cycle at high frequencies, this information is slew rate limited, and actual output level cannot be seen until the circuit comes to rest. After the circuit is finished counting, TTL level signals are present at these outputs. U3 is reset after the counting cycle is complete by a TTL reset signal at pin 3.

FIGURE 9-8A
COMPONENT LOCATOR
HIGH FREQUENCY (A106)



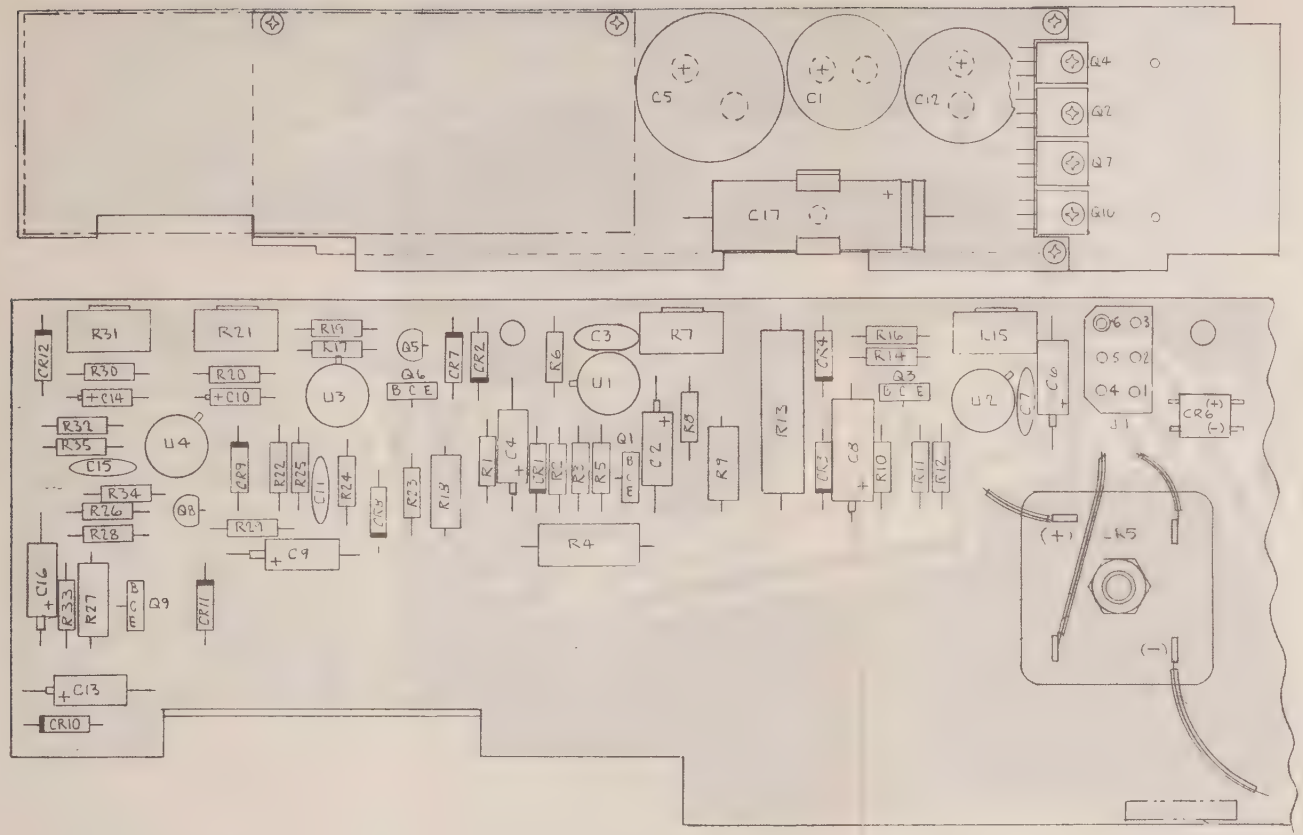
3 EIP P/N: 2710016.

4 INDUCTOR PART OF PC BOARD.

5 SELECTED AT TEST, NOMINAL VALUE SHOWN.

FIGURE 9-8B
SCHEMATIC DIAGRAM
HIGH FREQUENCY (A106)

048F



011D

POWER SUPPLY (A1/A107)

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two assembly groups:

(1) PC Board A107 contains the rectifiers, filter capacitors, and regulator circuitry.

(2) Chassis mounted components (A1-) consist of the power transformer (T1), primary wiring, fuse (F1), 115/230 power switch (S102), and the front panel POWER On/Off switch (S101).

Circuit Description

The basic voltages that are required by the counter are: unregulated +18 V, regulated +12 V, -12 V, +5 V and -5.2 V.

All the regulated voltages are produced by full wave rectifier and series regulator circuits. The +18 V unregulated voltage is also the input voltage for the +12 V regulator.

Each of the four regulator circuits contains an integrated circuit voltage regulator with current foldback capability, protective diodes, and provision for adjustment of the required output voltage.

The type of IC used in both the +12 V and +5 V regulators is an LM 305. This IC contains an internal temperature compensated voltage reference, as well as the necessary circuits to provide gain and current foldback limiting. The foldback current limit control resistors in the +5 V supply (for example) are R11, R12, and R13.

The negative supplies utilize an LM 304 as the basic IC regulator. This IC also contains an internal temperature compensated reference. To implement this reference an external pre-regulator is required. In the -12 V circuit (for example), the pre-regulator includes R22, R25, and CR9. Current foldback limiting uses internal IC circuitry in addition to R17, R18, R19 and Q5.

FIGURE 9-9A
COMPONENT LOCATOR
POWER SUPPLY (A107)

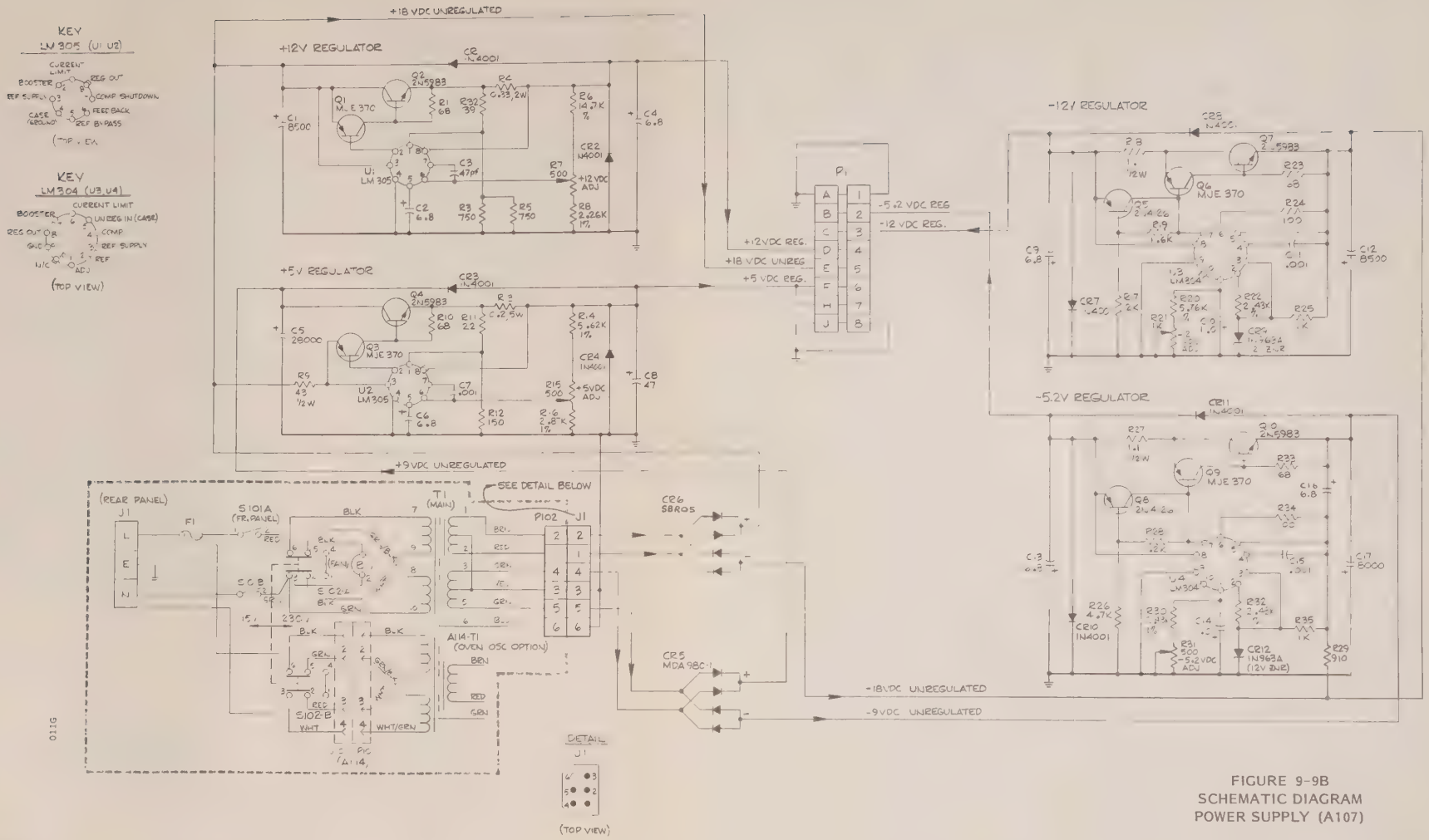
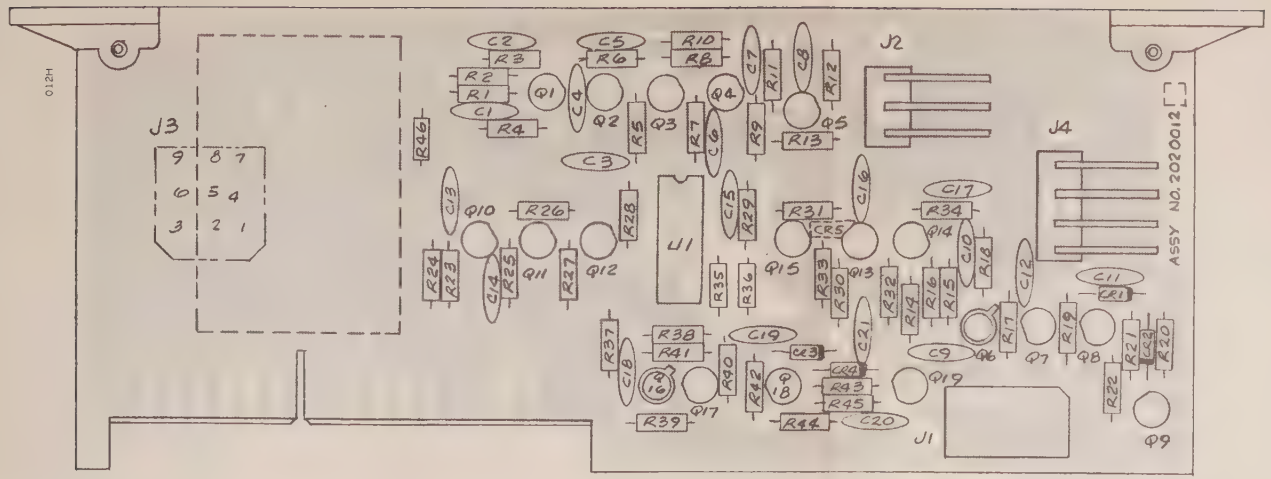


FIGURE 9-9B
SCHEMATIC DIAGRAM
POWER SUPPLY (A107)



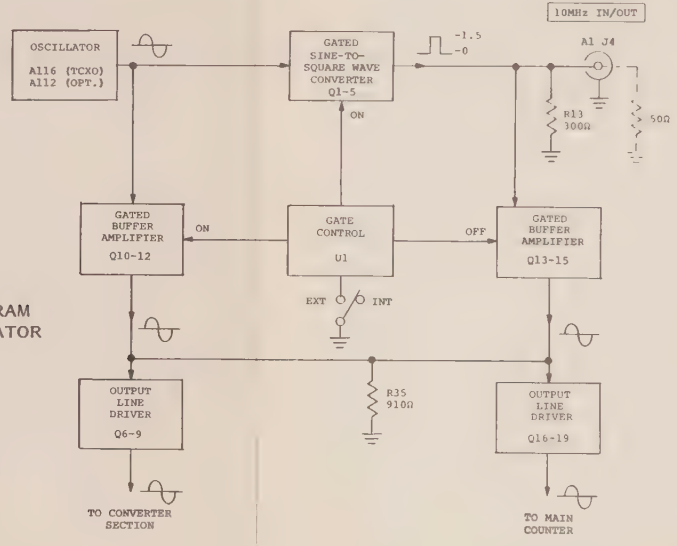


FIGURE 9-10C
FUNCTIONAL DIAGRAM
REFERENCE OSCILLATOR
BUFFER

FIGURE 9-10A
COMPONENT LOCATOR
REFERENCE OSCILLATOR
BUFFER (A108 + A116)

REFERENCE OSCILLATOR BUFFER (A108)

An internal temperature-compensated crystal oscillator — TCXO (A116), is used as the basic reference against which all input signals are compared. Additional time base options are available (see Section O - Options), which allow the user to select a level of precision compatible with measurement requirements. Specifications of the TCXO are listed in Section 3.

The counter may be operated from either the internal time base oscillator (TCXO or oven option), or from an external time base reference generator. Internal or external selection is made by means of a rear panel switch (A1S103). A rear panel BNC connector (A1J4) connects to A108J2 to furnish a 10 MHz square wave output signal, or accept a 10 MHz sine or square wave input signal (1 to 3 V p-p into 300 ohms). The method of switching between internal and external oscillators is shown in the Functional Diagram of Figure 9-10C. The power to the TCXO is switched on and off with the main counter power supply, while the power to any of the oven oscillator options remains on as long as the counter is plugged into an active power line, irrespective of the setting of the POWER On/Off switch.

Circuit Description

The TCXO sine wave is gated and converted to a TTL level in the circuit consisting of: a linear, low-gain isolation amplifier Q1; a differential sine-to-square wave amplifier Q2 and Q4; and an output current driver Q5. The gate function is accomplished by switching Q3 on and off through U1. Transistors Q10 - Q12, and Q13 - Q15, are identical sets of gated buffer amplifiers. Buffered gain is obtained in each set by the low-gain NPN/PNP pairs Q10/Q11, and Q13/Q14. The gating function is performed by switching Q12 and Q15 on and off through U1. Q6 - Q9, and Q16 - Q19, are identical sets of output line drivers. Low-gain, common emitter input stages Q6 and Q16 are followed by emitter followers Q7 and Q17, which drive push-pull emitter follower output pairs Q8/Q9, and Q18/Q19.

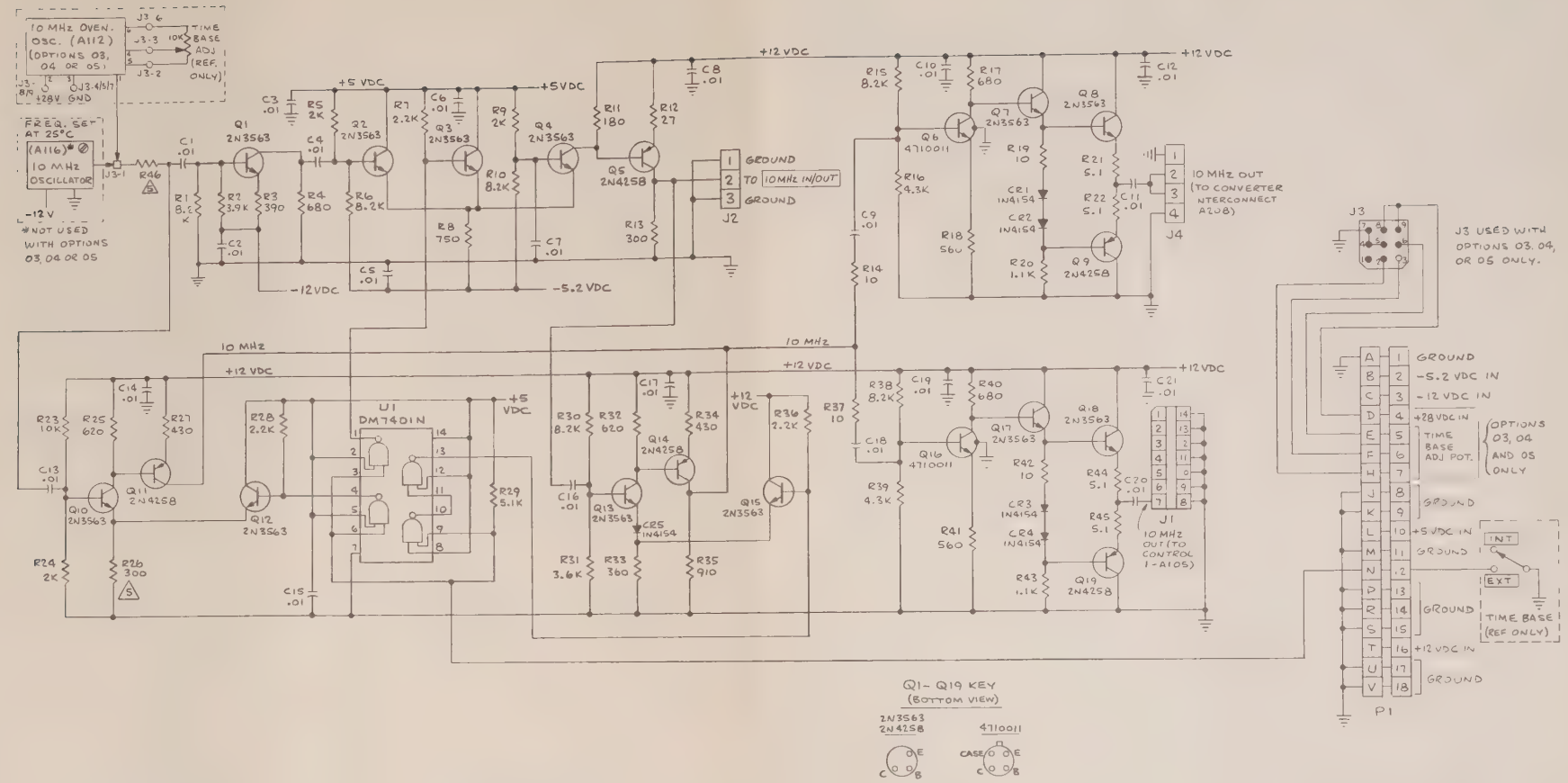
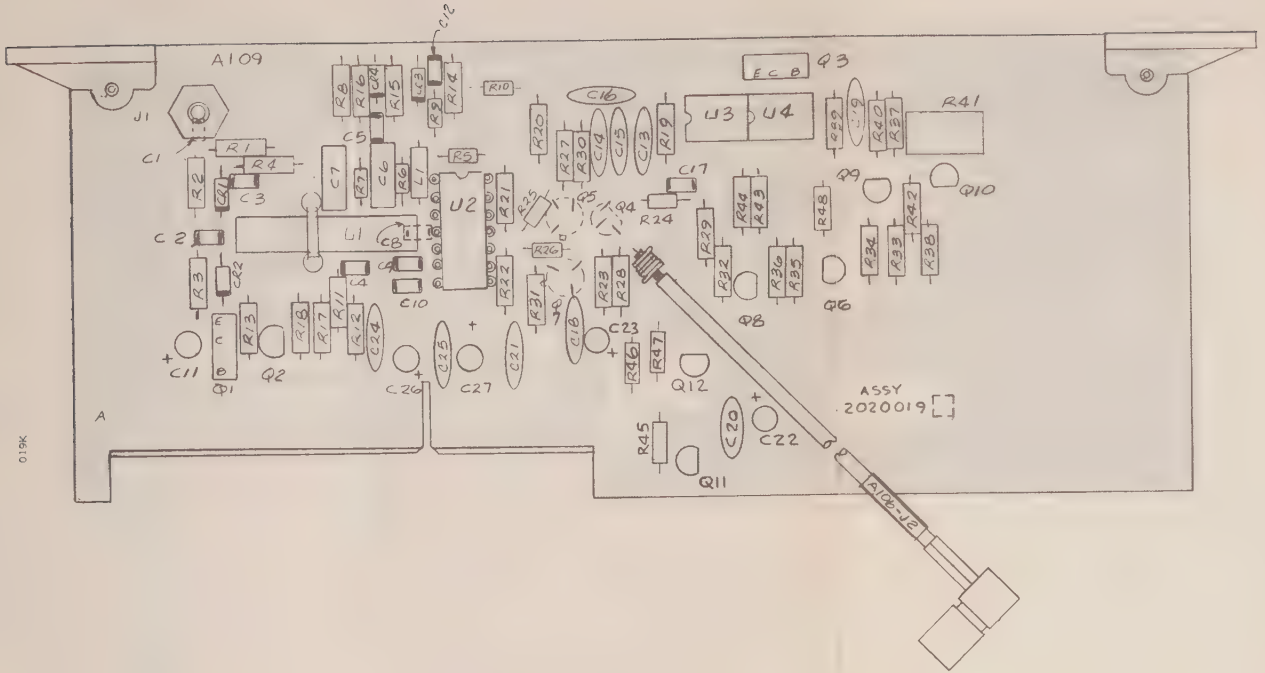


FIGURE 9-10B
SCHEMATIC DIAGRAM
REFERENCE OSCILLATOR
BUFFER (A108 + A116)



PRESCALER (A109)

This assembly permits the measurement of frequencies in the range of 100 MHz to 850 MHz, dividing the input frequency by a factor of four prior to counting. The counter then counts this scaled frequency with a gate time which has been expanded by four, thus yielding a direct frequency readout.

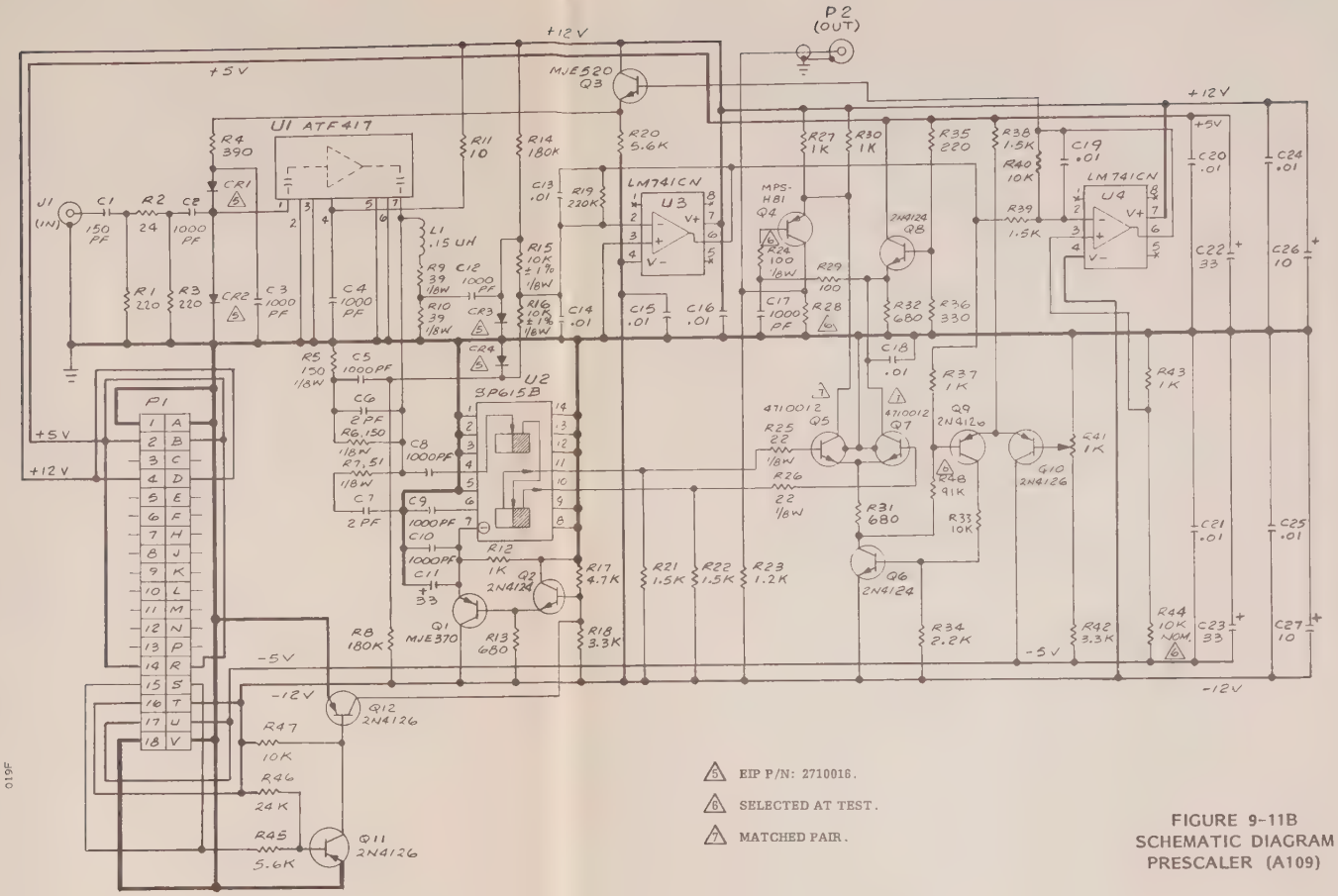
The major element of A109 is a ÷4 integrated circuit (U2). Sufficient drive level for this IC is provided by an integrated broad band amplifier U1. The output of U2 is amplified by the circuit consisting of Q4 through Q8.

Due to the tendency of U2 to free run with no input signal, it is necessary to disable the output if an input signal of sufficient amplitude is not present. This is accomplished with a threshold circuit consisting of a detector (CR3, CR4 and associated components), amplifier (U3), and differential trigger (Q9 and Q10). When the amplifier output applied to the base of Q9 exceeds the threshold level set by R41, Q9 turns on Q6 and thus enables the output amplifier.

In order to prevent U1 from overloading, automatic gain control is provided by comparing the amplified detector output to a preset level in U4 and feeding the output level back via Q3 to a pair of diodes CR1 and CR2. These diodes, when conducting, act to attenuate the input signal.

Transistors Q1 and Q2 form a -7 volt power source for U2.

FIGURE 9-11A
COMPONENT LOCATOR
PRESCALER (A109)

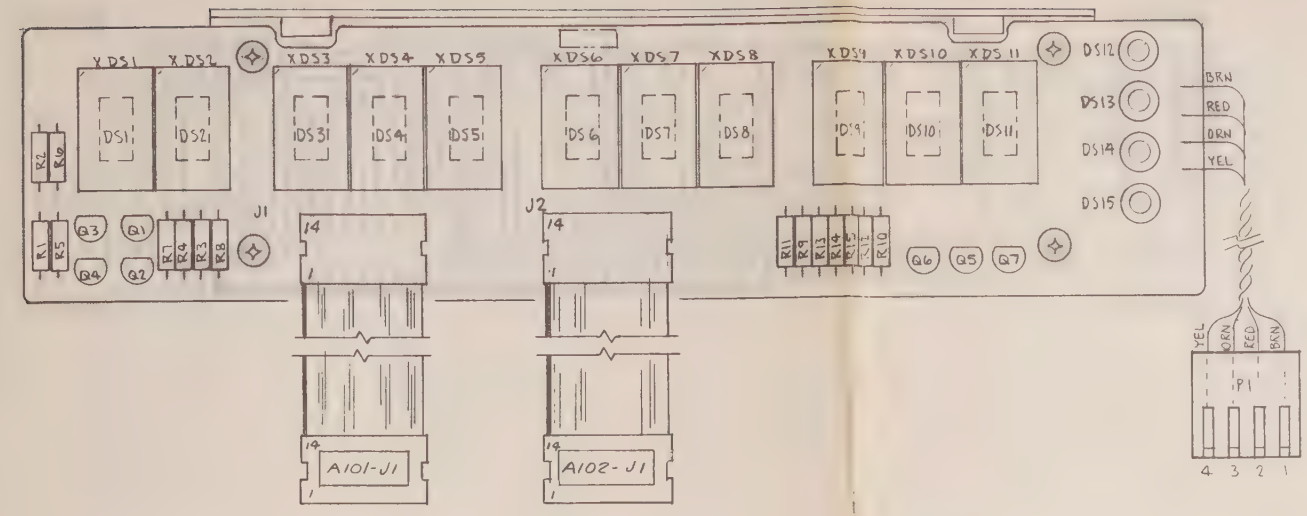


5 EIP P/N: 2710016.

6 SELECTED AT TEST.

7 MATCHED PAIR.

FIGURE 9-11B
SCHEMATIC DIAGRAM
PRESCALER (A109)



004A

DISPLAY (A110)

The Display Board (A110) contains eleven LED numerical display units mounted side-by-side, with spaces between each third digit from the right. The entire assembly is mounted behind a front panel window with the digits grouped to distinctly show GHz, MHz, kHz, and Hz. All drive signals for the Display are obtained from the Count Chain Boards (A101 and A102).

The digit displays are 7-segment LED's, with the anodes of each segment tied together. When the anode is at a positive voltage, grounding any cathode through its resistor illuminates that segment.

In this multiplexed system, the anode supply is applied in pulses (through anode drivers), which are synchronized with the cathode data to determine which segment shall light.

The segment drive is applied directly to the display digits. DS1-4, DS5-7, and DS8-11 have their corresponding cathode segments tied together within each group.

The selector drive to groups DS1, -5, -8, and DS2, -6, -9, are each driven by two transistors in parallel to meet the higher current requirements.

The remaining LED's use single transistor drivers. The drivers saturate when turned on, applying a voltage almost equal to the supply voltage for the display. This voltage is variable (by A103R22) for display brightness adjustment.

Four display lamps are included on this assembly, which illuminate to indicate GATE operation, Converter SEARCH, EXTernal REFerence, and REMOTE operation (Option 07).

FIGURE 9-12A
COMPONENT LOCATOR
DISPLAY (A110)

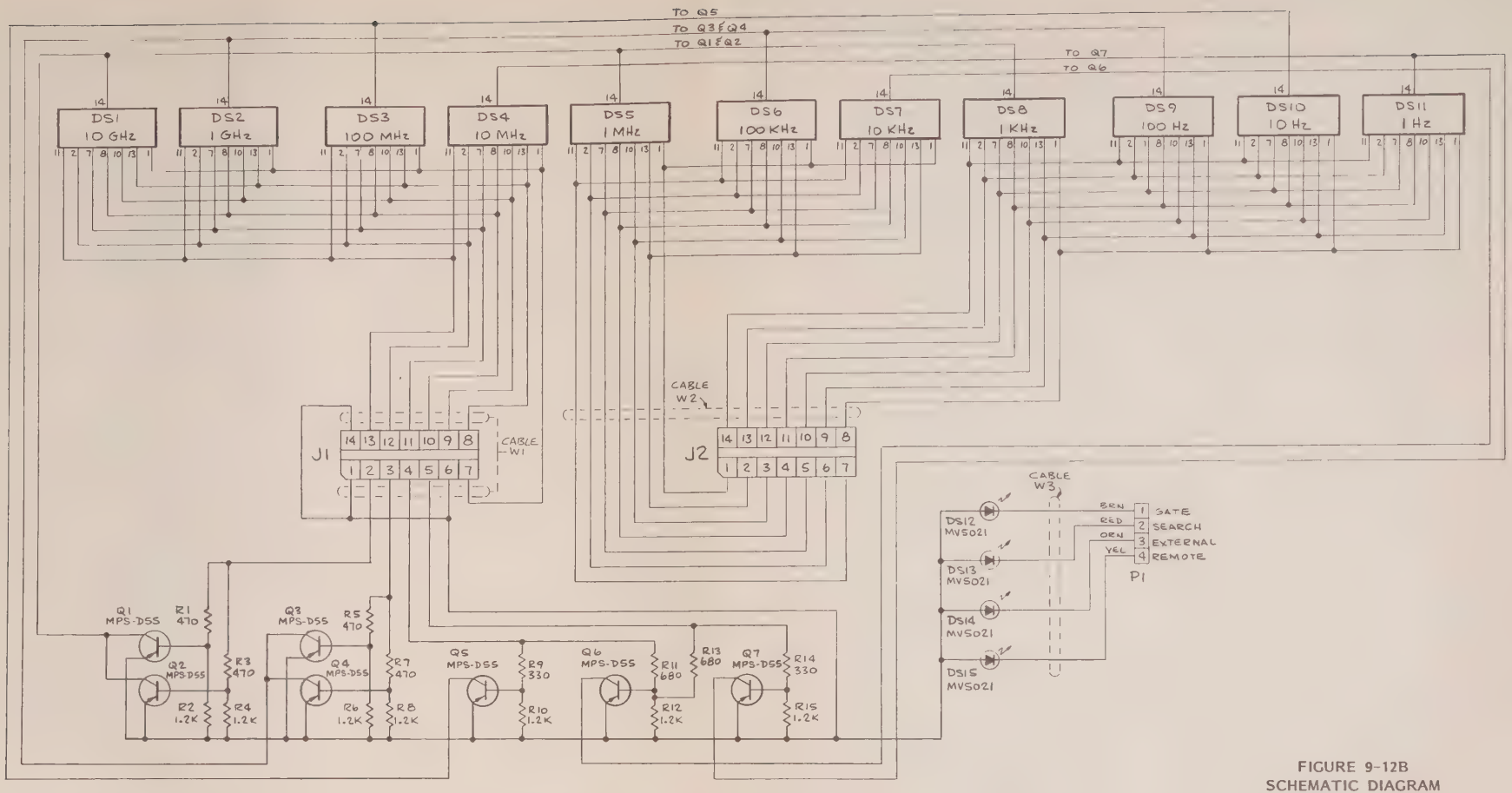
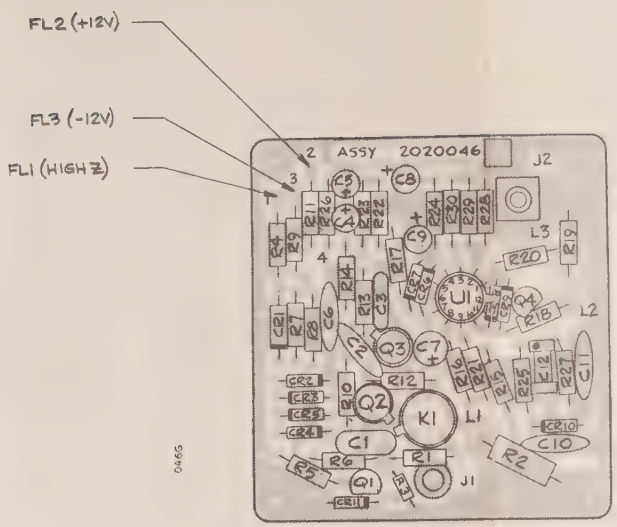


FIGURE 9-12B
SCHEMATIC DIAGRAM
DISPLAY (A110)



PREAMPLIFIER (A111)

The Preamplifier accepts Band I input signals at J1. The BAND SELECT switch controls relay K1 which selects either the Band IA high impedance (1 meg/20 pf) circuitry, or the Band IB low impedance (50 ohm) circuitry. The output of the Preamplifier (at J2) drives the High Frequency Board (A106).

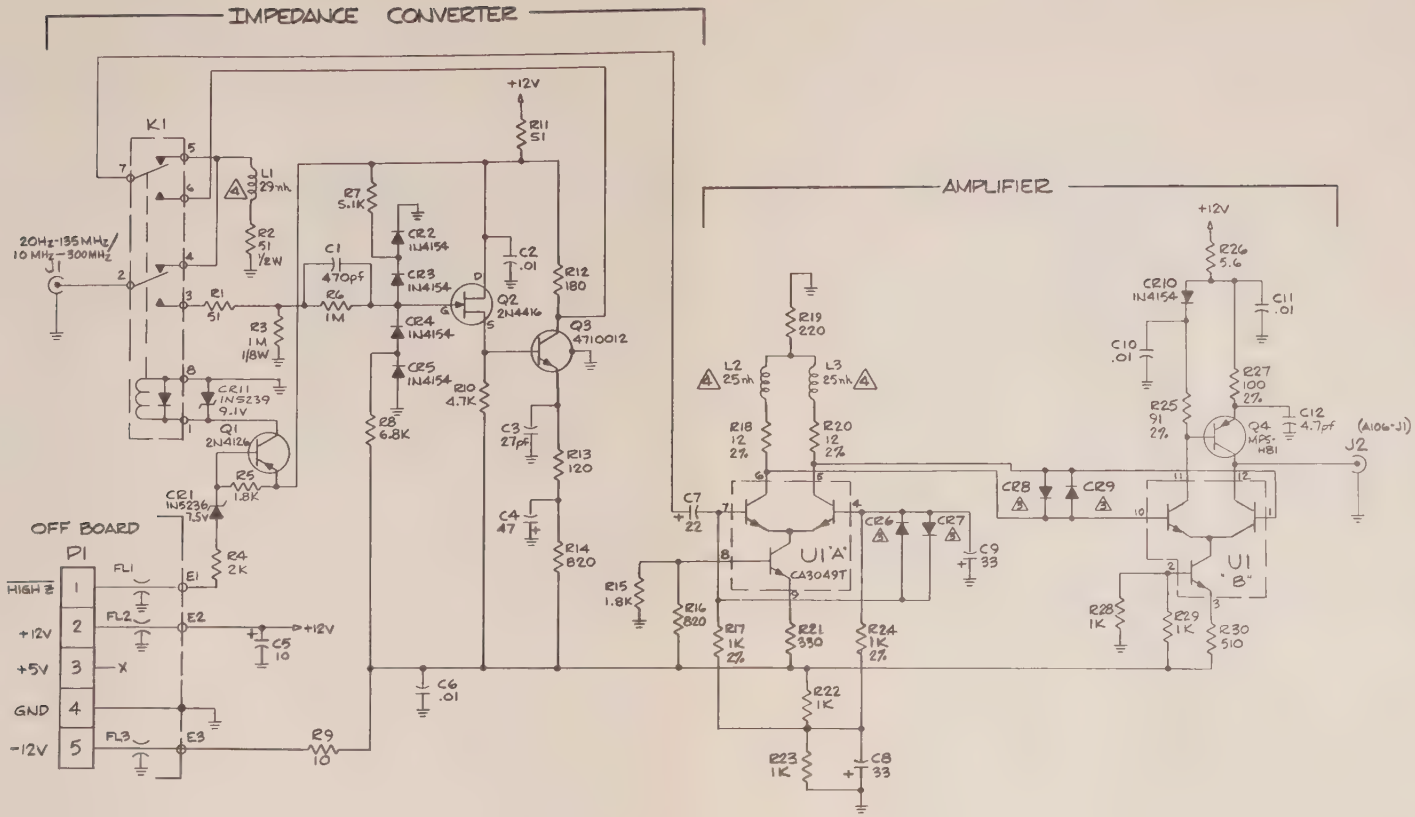
When K1 is de-energized, the amplifier operates in the 50 ohm mode. The terminating impedance is the parallel product of a 51 ohm resistor (R2) in series with a small inductance (L1), and the input impedance of the first amplifier stage (U1A). This combination keeps input VSWR below 1.5:1 up to 400 MHz. The signal is ac-coupled thru C7 to amplifier U1A, which is biased at approximately -6 Vdc. The collectors of U1A are operated against ground to minimize parasitic problems. Inductors L2 and L3 in series with load resistors R18 and R20, are high frequency peaking coils to flatten the response of the amplifier. R19 is used primarily to establish a dc voltage sufficiently negative to allow direct coupling to the second stage (U1B).

The output of the second stage is also operated against a ground reference. U1B pin 11 output is fed into current mirror Q4, whose output is then summed with the current of U1B pin 12, at J2. In this way, the two currents cancel, and only a small error component is left to generate an off-offset at the load.

When K1 is energized, the amplifier operates in the high impedance mode, with the relay routing the input signal to the impedance converter. The input impedance of the converter is essentially R3 in parallel with a network of components, and the gate of FET Q2. The net impedance of this combination is 1 megohm shunted by about 20 pf. The signal enters the gate of Q2 through diodes CR3 and CR4, which provide protective limiting for Q2. The limiter diodes are back-biased at about 0.7 V by networks R7/CR2 and R8/CR5. This back-biasing improves the frequency response by reducing the capacitance of CR3/CR4. The limiter is adequate to protect against an accidental connection of a 115 V, 60 Hz power line to the input, however, due to frequency compensating capacitor C1, this high voltage tolerance decreases as the frequency increases (see Specifications).

Q2 operates as a source follower to transform the impedance down to several hundred ohms. Q3 is a buffer amplifier with a gain of about 1.5; its purpose is to match the output of Q2 to the input of amplifier U1A, and to recover the loss of Q2 gain. The net gain through the Preamplifier is approximately equal for both high and low impedance inputs.

FIGURE 9-13A
COMPONENT LOCATOR
PREAMPLIFIER (A111)



3 P/N: 2710016.

4 INDUCTOR PART OF PC BOARD.

FIGURE 9-13B
SCHEMATIC DIAGRAM
PREAMPLIFIER (A111)

046D

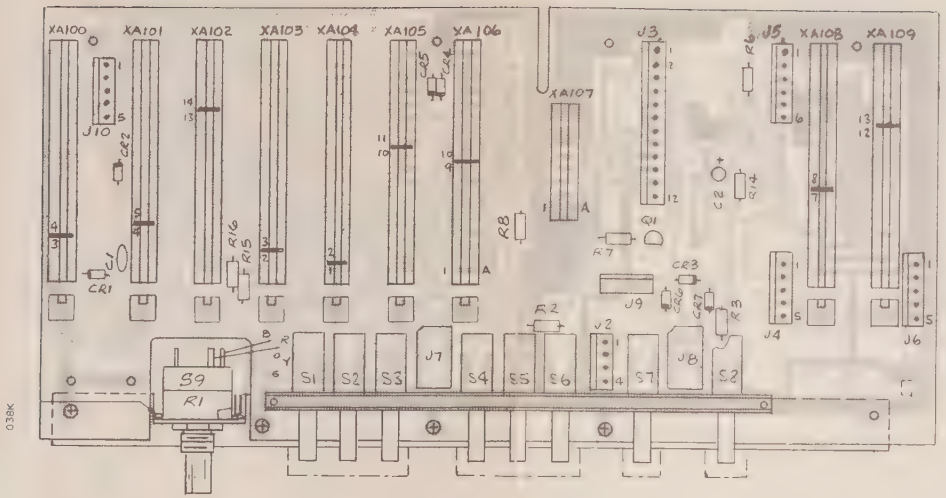


FIGURE 9-14A
COMPONENT LOCATOR
COUNTER INTERCONNECT (A113)

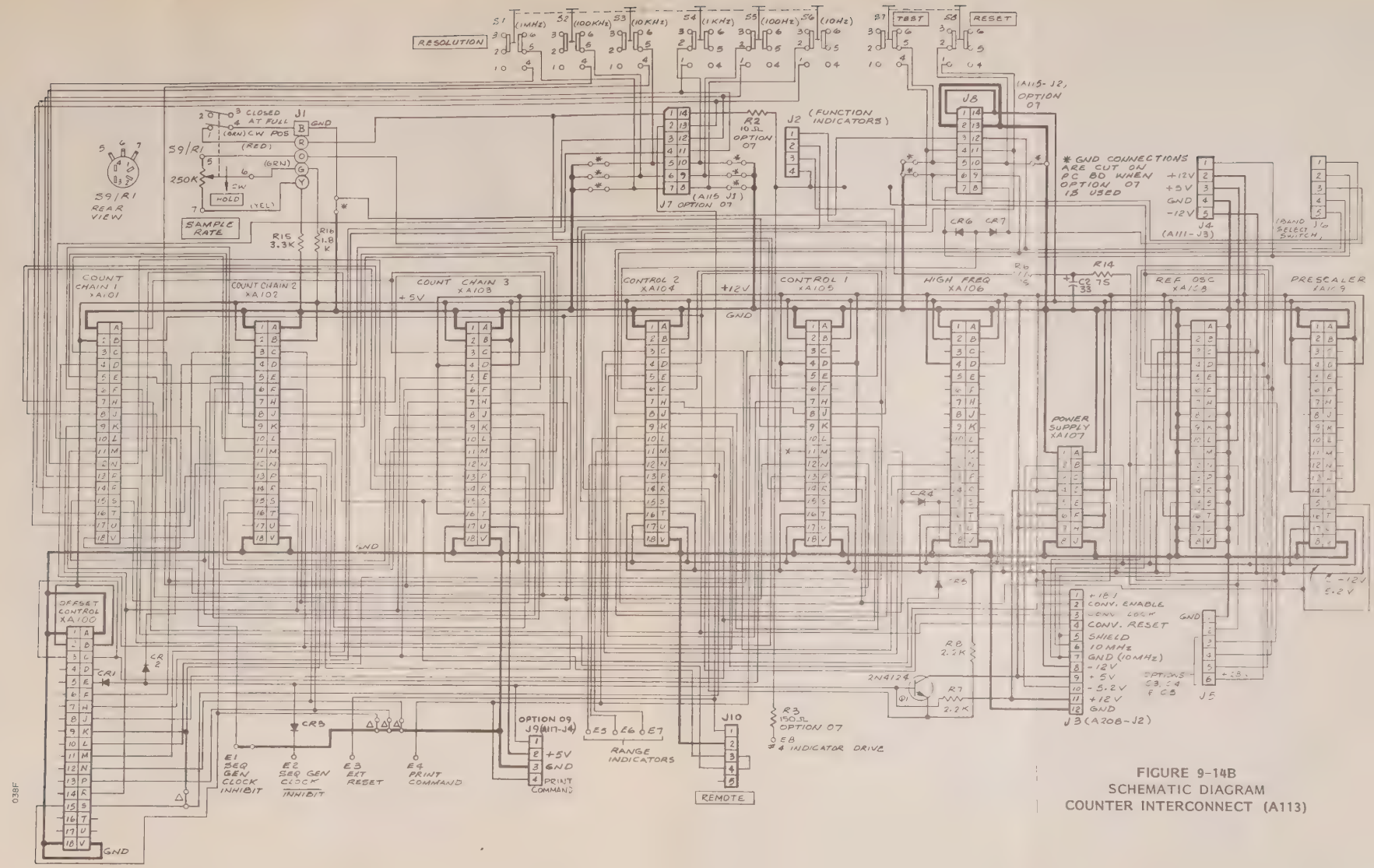
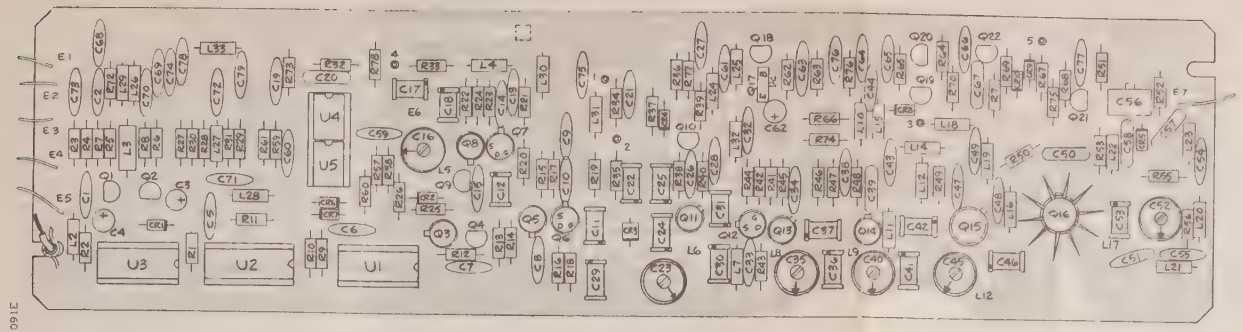


FIGURE 9-14B
SCHEMATIC DIAGRAM
COUNTER INTERCONNECT (A113)



TL60

SOURCE AMPLIFIER (A201)

General

A source of up to one watt of power at 200 MHz is required to drive the step recovery diode Comb Generator in YIG module A207. The 200 MHz must be both stable and coherent with the master oscillator in the counter. Stability is required to provide an IF spectrum that is dependent only upon the input signal spectrum. Coherence with the master oscillator is required to make counting accuracy dependent only upon the accuracy of the master oscillator.

The requirements of stability and coherence are satisfied by using a phase locked loop to lock a 200 MHz LC oscillator to the 10 MHz Time Base oscillator. The required output power is generated by a class C amplifier that contains a leveling loop to set the power output at any desired level from 1 mw to 1.1W.

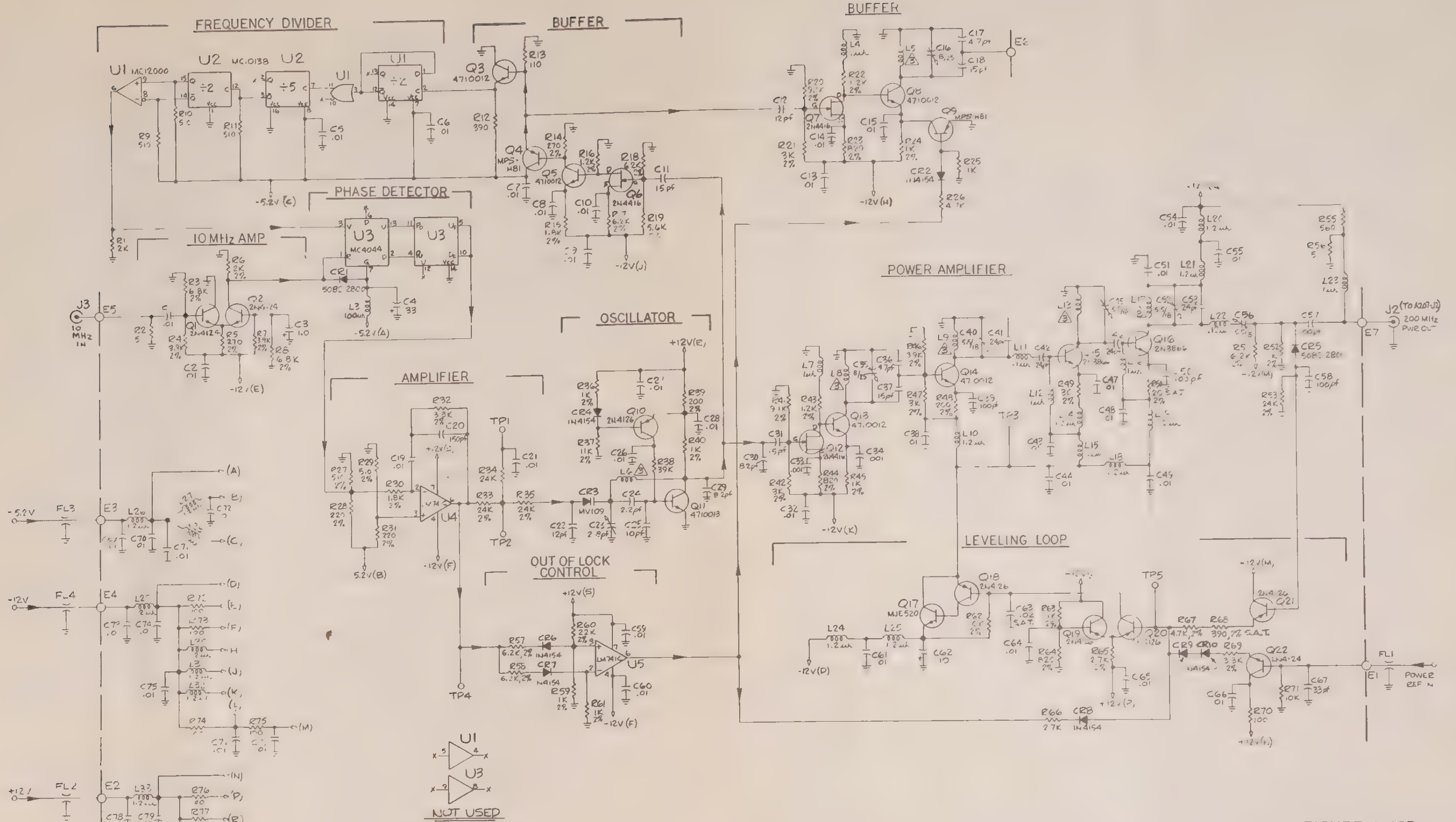
Circuit Description

The phase lock loop is a standard second order loop, implemented by using digital phase lock loop components. The 200 MHz LC oscillator is a modified Colpitts circuit with bias stabilization supplied by Q10. The output frequency of the 200 MHz oscillator is divided by 20 in U1 and U2 to produce a 10 MHz square wave. This signal is compared to the processed 10 MHz reference by phase detector U3. Phase error is amplified by active filter U4 and applied to voltage variable capacitor CR3. This holds the 200 MHz oscillator "locked" in phase to the 10 MHz reference signal. C23 sets the open loop center frequency of the oscillator.

The main power amplifier consists of four stages: Buffer amplifier Q12 and Q13, linear amplifier Q14, and two Class C stages Q15 and Q16. Output power level is controlled by adjusting the value of the negative voltage supplied by Q17 and Q18 to the linear amplifier and the Class C stages.

The power leveling loop operates by sampling the peak value of the output signal with CR5, and comparing this value to the Power Reference. The comparison is made by differential amplifier Q19 and Q20, which then controls Q17 and Q18.

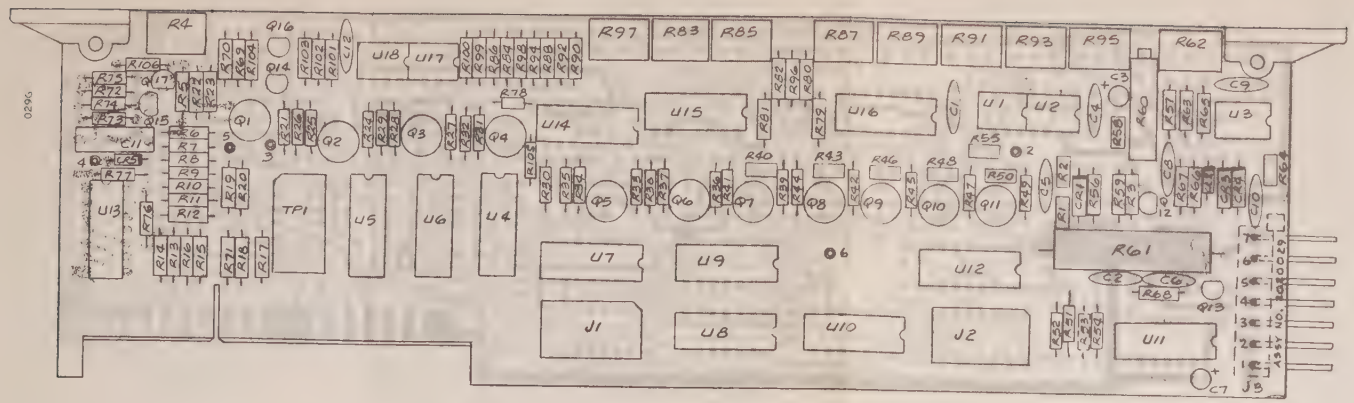
FIGURE 9-15A
COMPONENT LOCATOR
SOURCE/AMPLIFIER (A201)


FREQUENCY DIVIDER
BUFFER
PHASE DETECTOR
10 MHz AMP
OSCILLATOR
AMPLIFIER
OUT OF LOCK CONTROL
POWER AMPLIFIER
LEVELING LOOP
U1 MC12000
U2 MC10138
U3 MC4044
Q3 4710012
Q4 MPS-H81
Q5 4710012
Q6 2N4416
Q7 2N4416
Q8 4710012
Q9 MPS H81
Q10 2N4126
Q11 4710013
Q12 2N4416
Q13 47.0012
Q14 47 0012
Q16 2N3866
Q17 MJE520
J3 10 MHz IN
J2 (TO A207-J2) 200 MHz PWR OUT
POWER REF IN
-5.2V
-12V
+12V
FL3
FL4
E1
E2
E3
E4
E5
E7
TP1
TP2
TP3
TP4
TP5
U1
U3
NOT USED

△3 PART OF PC BOARD.

FIGURE 9-15B
SCHEMATIC DIAGRAM
SOURCE/AMPLIFIER (A201)

091B



CONVERTER CONTROL 2 (A202)

Converter Control 2 includes three circuit functions: one section comprising two Digital-to-Analog Converters (DACs), a Sweep Driver section, and a Power Control section. The DACs provide the ramp voltage for the Sweep Driver and the three most-significant-digit presets to the counting chain. The Sweep Driver supplies the drive current to tune the YIG Filter within A207. The Power Control section programs the amount of RF power delivered to the Comb Generator portion of A207.

Digital-to-Analog Converter Section

This section consists of a clock generator, two digital-to-analog converters: DAC 1 and DAC 2, and logic circuits to control the clock generator and the two DACs. The DACs provide the ramp waveform that is used to control the YIG Filter. The ramp, in turn, is controlled by the clock. DAC 1 step size is 200 MHz at a rate of one step per millisecond. DAC 2 step size is 2 MHz at a rate of two steps per milliseconds.

When the YIG Filter is locked onto a comb line, the number in DAC 1 is preset into the three most-significant-digits of the Counting Chain.

Clock pulses are generated by the unijunction oscillator circuit of Q15, and clamped to TTL level by CR5 and the voltage divider formed by R76 and R77. The NAND gates of U13 to enable DAC 1 or DAC 2 and disable the clock upon command from Converter Control 1 (A203). Q14 provides a negative current step whenever DAC 2 is enabled. This compensates for the time delay between current and magnetic field within the YIG structure. This delay is the result of eddy currents generated by a changing magnetic field.

Clock pulses are converted into a ramp by successively summing in a larger amount of current each time a clock pulse occurs. One side of each summing resistor is connected to the inverting input of U2. Each resistor will then sum in current whenever the other side of the resistor is returned to a reference voltage. For the 2 MHz to 40 MHz steps, the resistors are effectively connected to the +5 V supply when their associated decade counter output goes to a logic "1". For the 80 MHz to 20 GHz steps, the logic 1 outputs saturate the associated switch transistor, thus effectively connecting the resistor between the +3.1 V reference supply and the U2 input. The amount of current added is carefully regulated by the tight tolerance of the summing resistors, and the temperature compensated reference voltage supplied by CR1 and U1.

DAC 1 controls the steps from 200 MHz to 19.8 GHz; DAC 2 from 2 MHz to 198 MHz. U4 generates a reset pulse when DAC 2 reaches 198 MHz; U11 will generate a reset pulse when DAC 1 reaches a specific step in the ramp, determined by the position and/or selection of resistors R51 through R54. The three most-significant-digit information is sent to Count Chain 2 (A102) via connector J2. Connector J1 provides inputs to YIG Preset Options 01 and 02 (see Section O), which initiate the ramp starting point at a non-zero frequency.

Sweep Driver Section

The Sweep Driver section consists of an operational amplifier, a voltage translator, and two cascaded output transistors. The second output transistor (A2Q1) is mounted on the Converter chassis.

The ramp from the DACs drives the inverting input of of U3. R62 sets the ramp offset, and R60 determines the slope of the ramp. Feedback voltage is obtained across sense resistor R61, forcing an extremely linear relationship between the sweep voltage and the YIG Filter current. CR4 limits the voltage developed across the YIG Filter tuning coil during flyback, in order to protect transistors Q13 and A2Q1.

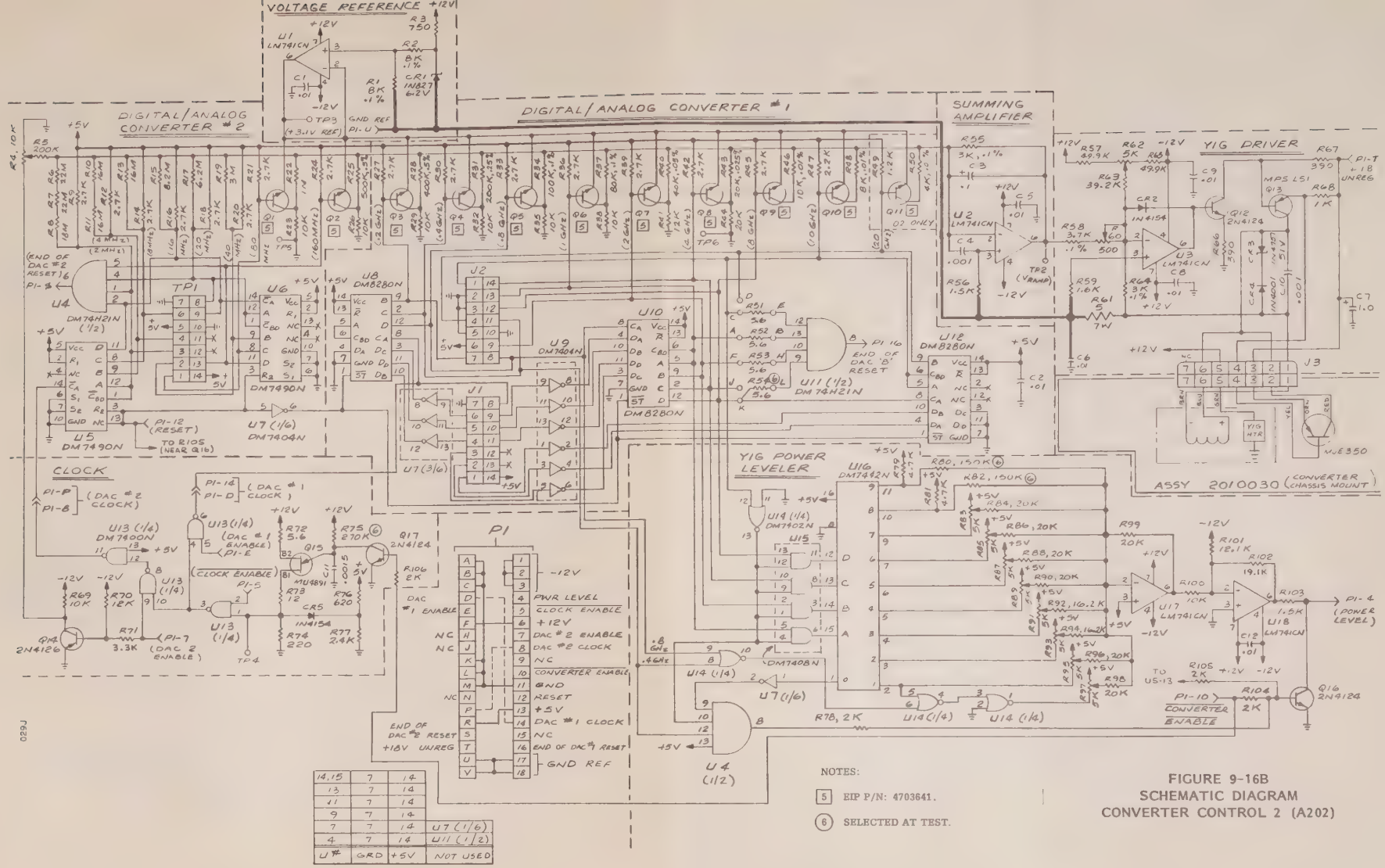
Power Control Section

The Power Control circuit provides the means for reducing the power output of the Comb Generator during the sweep period from 1 to 9.8 GHz. This limits the maximum amplitude of spurious signals generated in the Mixer. This power reduction is accomplished by varying the output level of the Source/Amplifier (A201) with the control voltage produced by the Power Control Section.

The digital information which controls DAC 1 is fed to U16, a BCD-to-decimal decoder. The output at P1 pin 4 will be a series of steps, each step covering five comb lines from 1 to 9.8 GHz. U14 is used to give an extra step between 1.4 and 1.8 GHz. By proper adjustment of each step, the power into the Comb Generator can be programmed to provide relatively constant comb line power at the Mixer diode.

When the Counter is set to Band I or Band II, the power level control voltage is held at minimum by turning on transistor Q16.

FIGURE 9-16A
COMPONENT LOCATOR
CONVERTER CONTROL 2 (A202)



14,15	7	14	
13	7	14	
11	7	14	
9	7	14	
7	7	14	U7 (1/6)
4	7	14	U11 (1/2)
U#	GRD	+5V	NOT USED

FIGURE 9-16B
SCHEMATIC DIAGRAM
CONVERTER CONTROL 2 (A202)

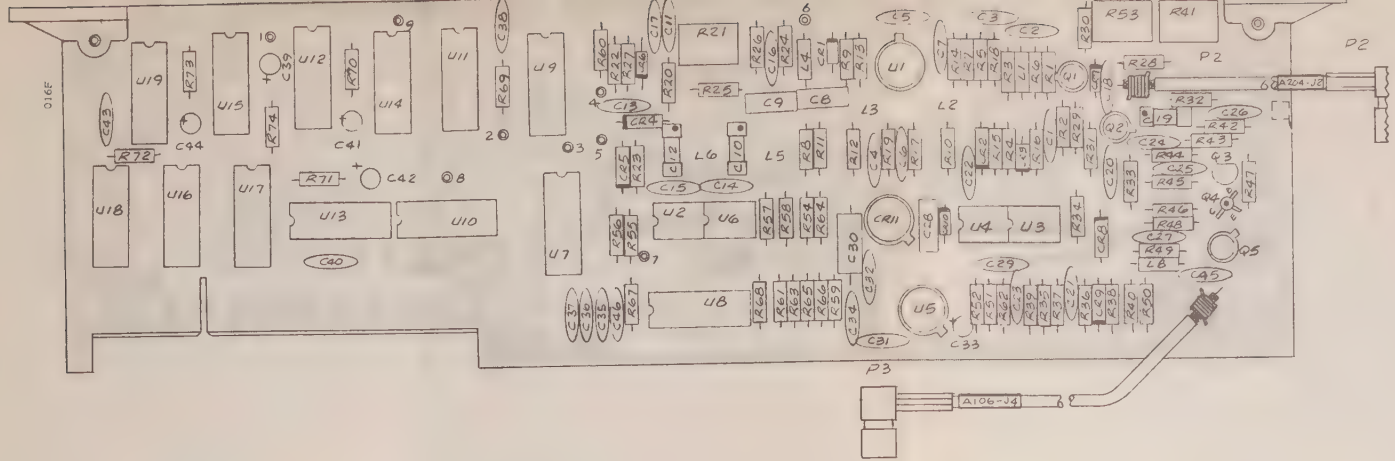


FIGURE 9-17A
COMPONENT LOCATOR
CONVERTER CONTROL 1 (A203)

CONVERTER CONTROL 1 (A203)

Converter Control 1 performs all the control functions necessary to lock the microwave Converter to the correct YIG/Comb Generator (A207) output frequency, and provide appropriate signals to the direct counter.

Converter Control 1 consists of five basic functional sections: a Video Limiter, a Video Detector, an In-Band Detector, an Analog Processor, and Signal Acquisition Logic. The Video Limiter processes the signal from A204 to provide a constant amplitude signal to the High Frequency Board (A106). The Video Detector converts the incoming video signal from A204 to a level proportional to the incoming power. This signal is then compared to a number of preset levels in the Analog Processor circuits, and converted into digital signals for further processing. The In-Band Detector is used to determine whether or not the video frequency falls within the desired passband, and to enable the Analog Processor circuits. The Signal Acquisition Logic provides the digital commands to control the sweep circuits and to lock the Converter on the appropriate comb line.

Figure 9-17C shows the operating sequence of the Converter. In the absence of an input signal to the Converter, a 200 MHz/ms sweep is continuously generated (DAC 1 ENABLE and CLOCK ENABLE are high). At the end of each sweep, a CONVERTER RESET command is generated (point A to point B on waveform). When a signal is applied, a Video Detector output will be generated when the YIG Filter is tuned through the correct harmonic (point C). When this signal appears, a CONVERTER RESET command is again generated (point C to point D), and the sweep is reset to zero. A new sweep is initiated (point D) and eventually the Video Detector again produces an output (point E). At this point, a small backward step will be taken, followed by a 3 millisecond delay (point E to point F). At the end of this time, DAC 2 turns on, and a considerably slower sweep (4 MHz/msec) begins. At point G, the Video Detector output has reached 90% of the value stored in the Peak Detector, and the sweep is stopped. Three milliseconds later (point H), a LOCK command is given, which will allow the counter to read the frequency applied to the High Frequency Board (A107). If the sweep is inhibited from stopping at point G (by grounding A203TP4), the Video Detector output will appear as shown by the dotted line on the waveform.

Video Limiter and Video Detector Sections

The incoming signal from the Video Amplifier (A204) enters at connector P2, passes through an isolation buffer Q2, and is limited by the differential amplifier Q4-Q5. This provides a fixed output amplitude of approximately 1 V peak-to-peak to the High Frequency board. Q2 also drives the Video Detector diode CR8. Diode CR9 (matched to CR8) is used for temperature compensation of CR8 bias. The rectified signal is then amplified by U3, whose gain is set by Video Detector Gain Control R41. The setting of R41 determines the minimum required lock signal from the Video Amplifier. As such, its setting plays an important part in determining the sensitivity of the Converter. Refer to Section 6 for the proper adjustment procedure.

In-Band Detector

The Video Amplifier also drives an additional buffer Q1, which provides the drive signal for a two-stage limiter U1. This limiter drives a bandpass filter, whose output is then detected by CR4. Matched diode CR5 provides temperature compensation for CR4. The output level of CR4 thus is a function of frequency only. When the output of CR4 exceeds the DC level set by R21, the In-Band Detector triggers, generating a TTL compatible output signal. Trigger level hysteresis prevents the In-Band Detector from turning off until the signal is reduced considerably in power. R21 is set to turn on the In-Band Detector at 250 MHz. Once turned on, it will not turn off until the frequency is increased to approximately 275 MHz. It is this difference in turn-on and turn-off frequency, which determines the FM tolerance of the heterodyne Converter at the edge of the video passband.

Analog Processor

The Analog Processor contains an AC-coupled comparator, a DC-coupled comparator, and a peak detector. The purpose of this section is to convert the analog output of the Video Detector into digital commands which can be used to lock the Converter to the correct comb line. U8 compares the Video Detector output to preset levels. U8A is AC-coupled, and therefore requires that the Video Detector signal be sweep related in order to trigger. U8B is DC-coupled, and is used to determine that there is sufficient power level coming from the Video Amplifier. Both comparators are enabled by the In-Band Detector output.

Operational amplifiers U4 and U5 and their associated circuitry form a peak detector, which stores the maximum Video Detector output during a particular sweep period. U7 compares the stored output of the peak detector with the instantaneous value of the Video Detector output. Switching occurs when the Video Detector output reaches 90% of the stored peak.

The Peak Detector is discharged by U6. A CONVERTER RESET Command or lack of the In-Band Detector signal will activate U6. The circuit is inhibited from discharging by the presence of the DAC 2 ENABLE discussed below.

The outputs of each of the three comparators U8A, U8B, and U7, then form input commands to the Signal Acquisition Logic section.

Signal Acquisition Logic

There are five commands generated by the Signal Acquisition logic: CONVERTER RESET, DAC 1 ENABLE, DAC 2 ENABLE, CLOCK ENABLE, and LOCK. The CONVERTER RESET command is a 5 millisecond pulse used to reset the digital logic on both this board and Converter Control 2 (A202). The three enable commands determine which DAC, if any, will control the sweep current applied to the YIG Filter. If the CLOCK ENABLE is low, no sweep will occur, and the current into the YIG Filter will remain constant. If the CLOCK ENABLE is high, either DAC 1 or DAC 2 (on Converter Control 2) will generate a current sweep. The appropriate DAC is selected by the DAC ENABLE commands.

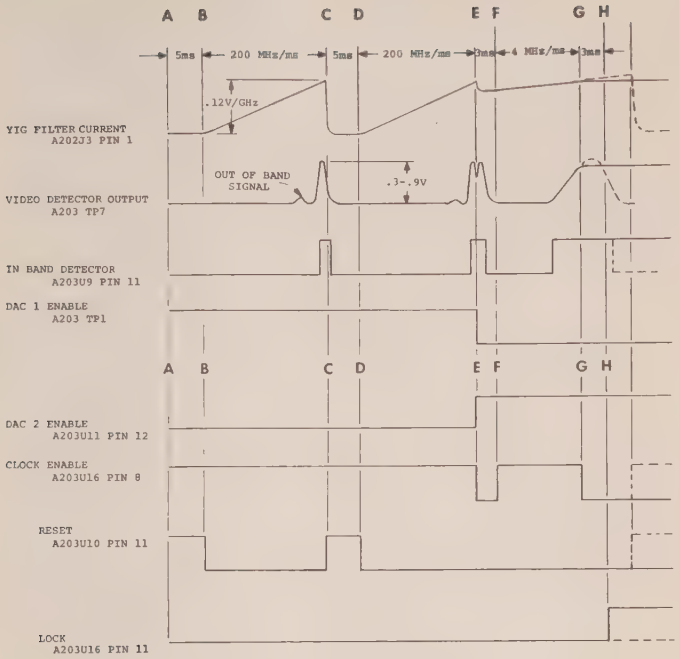


FIGURE 9-17C
OPERATING SEQUENCE
CONVERTER CONTROL 1 (A203)

The following description is keyed to the corresponding lettered points on the waveforms shown in Figure 9-17C.

A. Initiation of CONVERTER RESET: A CONVERTER RESET will occur in the digital logic whenever any one of the six inputs of the hex inverter U18 goes high. When this occurs, pin 2 of multivibrator U19 goes low, causing it to generate a 5 millisecond CONVERTER RESET pulse. This pulse will reset DAC 1, DAC 2, U14B, and U17A. Events that will initiate a CONVERTER RESET are: (1) CONVERTER RECYCLE command from A104. (2) Either DAC reaching the end of its range. (3) Loss of sufficient video level (U8B input drops below threshold). (4) Image rejection circuit operating (refer to explanation in later paragraph).

B. Start Sweep: CONVERTER RESET goes low and enables U11B.

C. Presence of Sweep Related Signal: An In-Band signal of sufficient amplitude triggers U8A. When the signal drops below the threshold value, the negative transition triggers flip-flop U11B. This action triggers U14B, generating a CONVERTER RESET. All circuits except U11B are reset; U14A is enabled.

D. Start of Second Sweep: End of CONVERTER RESET triggers U14A which, in turn, enables U11A. The purpose of the second sweep is to guarantee that after the signal has been applied to the Converter, a sweep is begun from zero frequency. This prevents locking to a harmonic of the input frequency.

E. Presence of Sweep Related Signal: The negative transition of U8A, as described in paragraph C, triggers U11A. This turns off DAC 1 ENABLE, and turns on DAC 2 ENABLE. In addition, multivibrator U13 is triggered, which generates a 3 millisecond pulse. The CLOCK ENABLE is turned off during this pulse, and U17A is triggered. The output of U17A enables U17B. The loss of the DAC 1 ENABLE also results in a negative current step (generated on Converter Control 2) such that the YIG Filter is tuned back through the frequency that initiated the trigger. This action causes the twin peaks in the Video Detector output. During this period, the Peak Detector has stored the peak detected signal level; the voltage at U7 pin 5 is 90% of that peak.

F. Start of DAC 2 Sweep: The CLOCK ENABLE command goes high at the end of the pulse from U13.

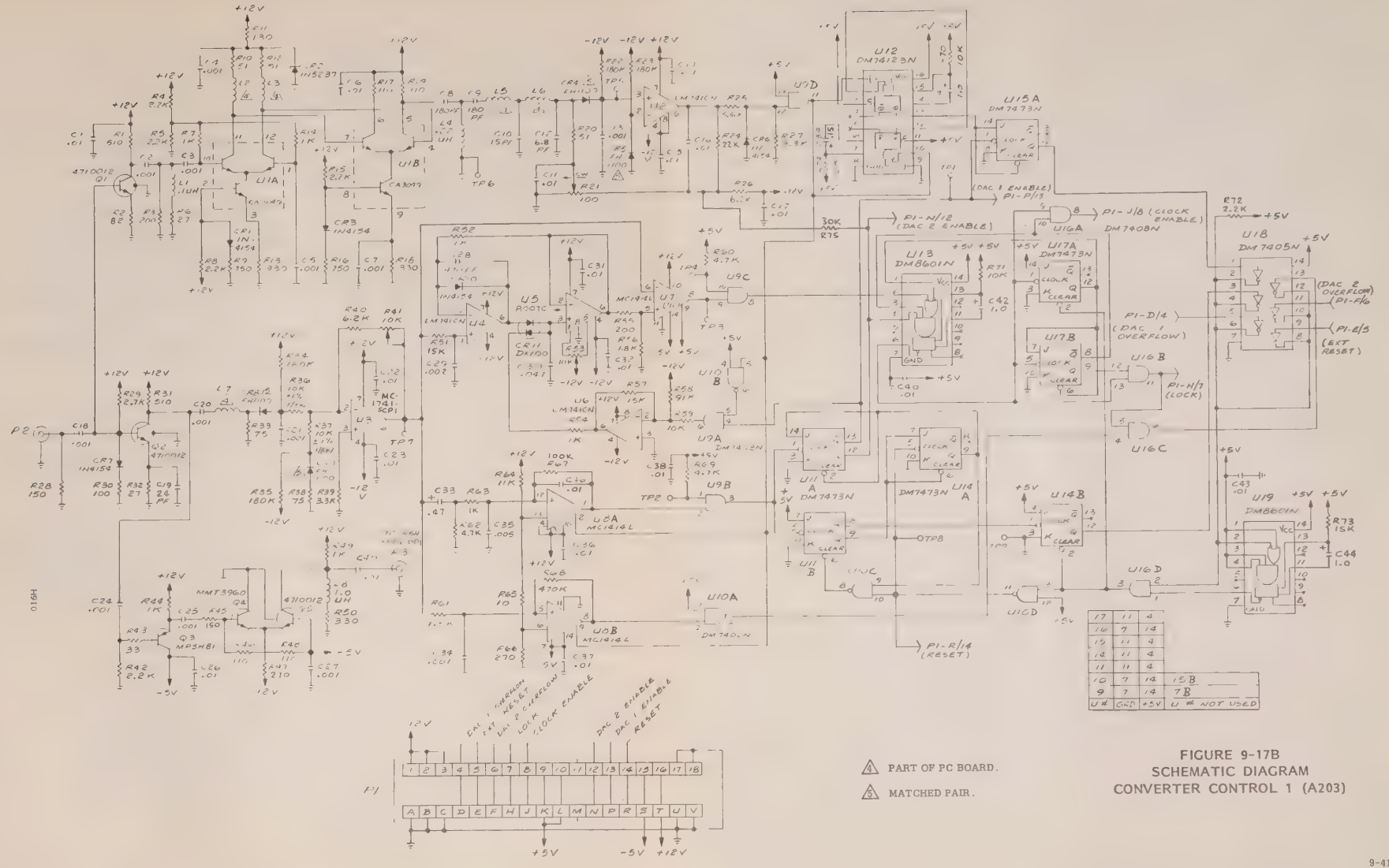
G. Stop Sweep: When the Video Detector output reaches 90% of the stored peak, U7 is triggered which again causes a 3 millisecond pulse to be generated by U13. This pulse triggers U17B which disables the CLOCK ENABLE.

H. Lock: At the end of the 3 millisecond pulse, the LOCK command is obtained at U16 pin 11; this allows the counter to display the input frequency. If at any time after LOCK command occurs, the output of the Video Detector should drop below the threshold set at U8 pin 6, a CONVERTER RESET command will be initiated when U16 pin 6 goes high.

Image Rejection

At input levels below the specified sensitivity, it is possible that although the video level is insufficient to trigger U8A on the correct comb line, the next higher line is sufficient. If the counter should lock to this line, called the image, an erroneous reading would result. To prevent this, an image rejection circuit consisting of U12 and U15A is provided.

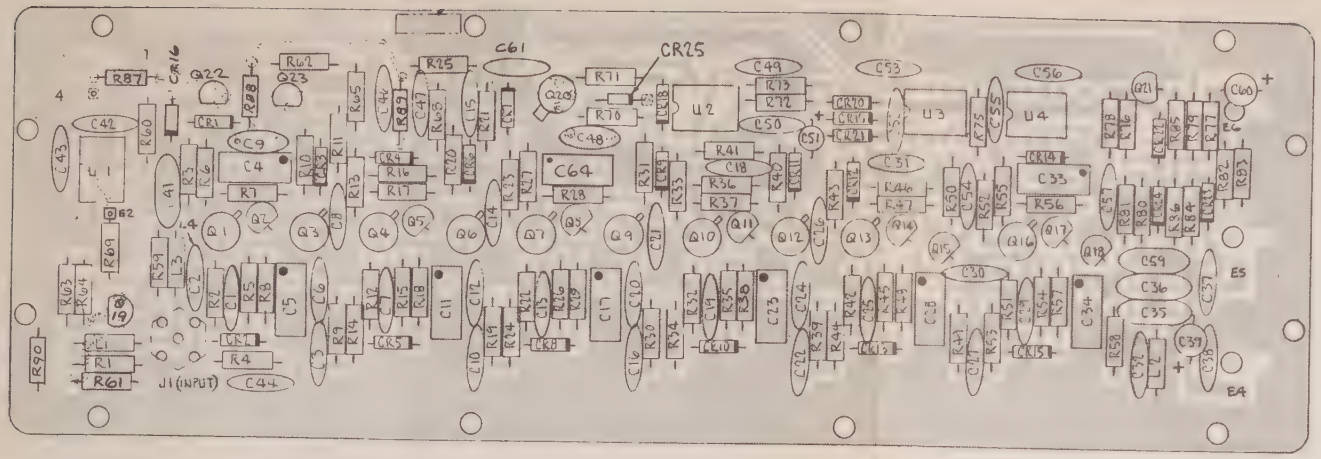
If the In-Band Detector turns on, then off, without U8 triggering, multivibrator U12 enables the flip-flop U15A for 3 milliseconds. If during this period, U8 is triggered, resulting in DAC 1 ENABLE going low, U15 will be triggered, resulting in a CONVERTER RESET. The Converter will thus fail to lock on the image.



4 PART OF PC BOARD.

5 MATCHED PAIR.

FIGURE 9-17B
SCHEMATIC DIAGRAM
CONVERTER CONTROL 1 (A203)



014J

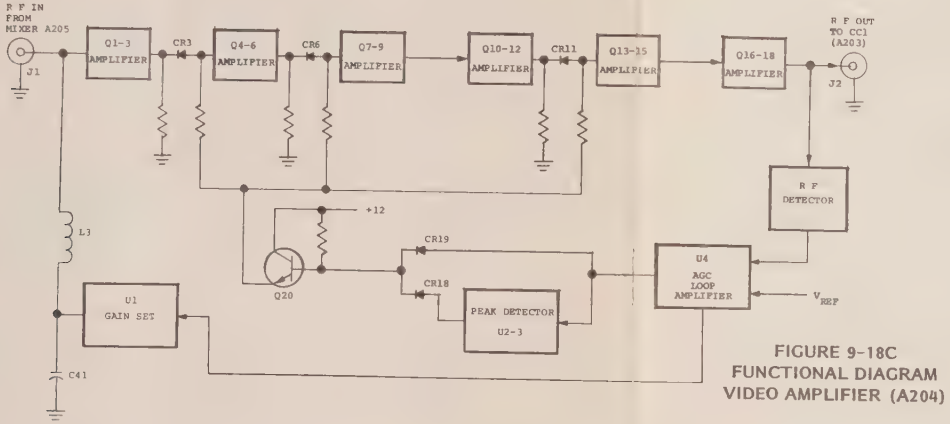


FIGURE 9-18C
FUNCTIONAL DIAGRAM
VIDEO AMPLIFIER (A204)

VIDEO AMPLIFIER (A204)

The difference frequency generated in the Mixer (A205) is applied to the input connector J1 of the Video Amplifier. The amplified output at J2 is sent to Converter Control 1 (A203) for further processing.

The circuitry consists of six essentially identical gain blocks and an automatic gain control circuit. Overall gain of the unit is nominally 56 dB with a frequency range of 25 MHz to 275 MHz. A block diagram of A204 is shown in Figure 9-18C.

Each gain block includes a broadband feedback pair Q1-Q2, an emitter follower Q3, band shaping C4-C5, and bias circuitry. Overall gain per block is approximately 10 dB.

The normal gain control circuit consists of a level detector composed of CR23 and CR24, the loop amplifier U4, PIN current driver Q20, and PIN attenuator diodes CR3, CR6, and CR11.

Once this loop has turned on, a memory circuit serves to hold the gain reduced for a period of time. This is to assist in the centering of the YIG Filter passband on a comb line as discussed under Converter Control 1 (A203). This circuit consists of the peak detector formed by U2, U3, and associated elements. Gate diodes CR18 and CR19 give control of the agc system to the lowest of the outputs of U2 or U4.

The remaining circuitry on A204 reduces the maximum available gain at high RF power levels (greater than -10 dBm). The DC output current (negative) from the Mixer is a measure of RF input power. As this current increases the output from U1 increases from its initial value of -7.5 volts towards 0 volts. This varies the level at which Q21 turns on, which, in turn, sets the maximum output of U4. Q19 forms a clamp so that there is a limit as to how far the gain may be reduced.

FIGURE 9-18A
COMPONENT LOCATOR
VIDEO AMPLIFIER (A204)

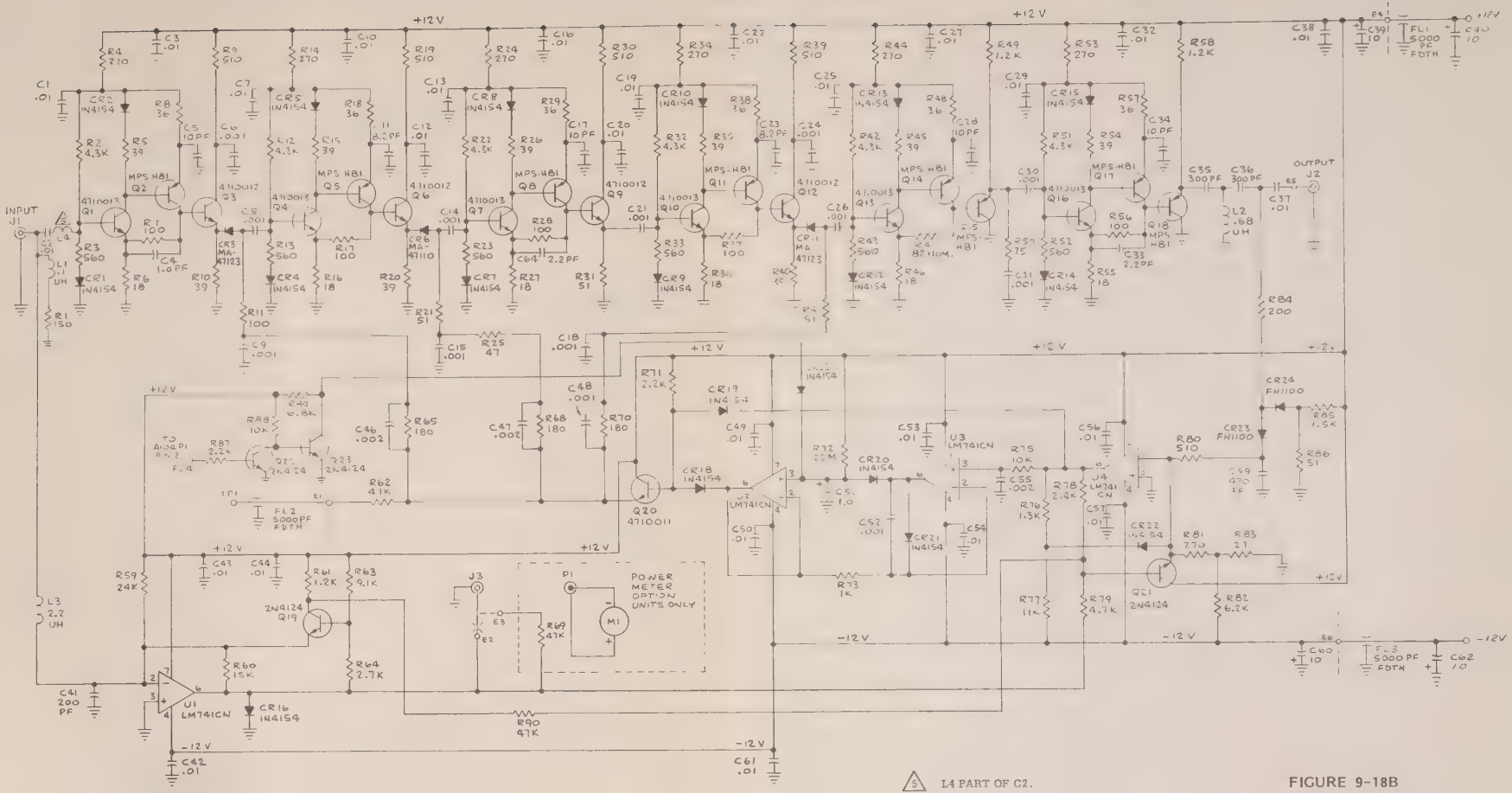
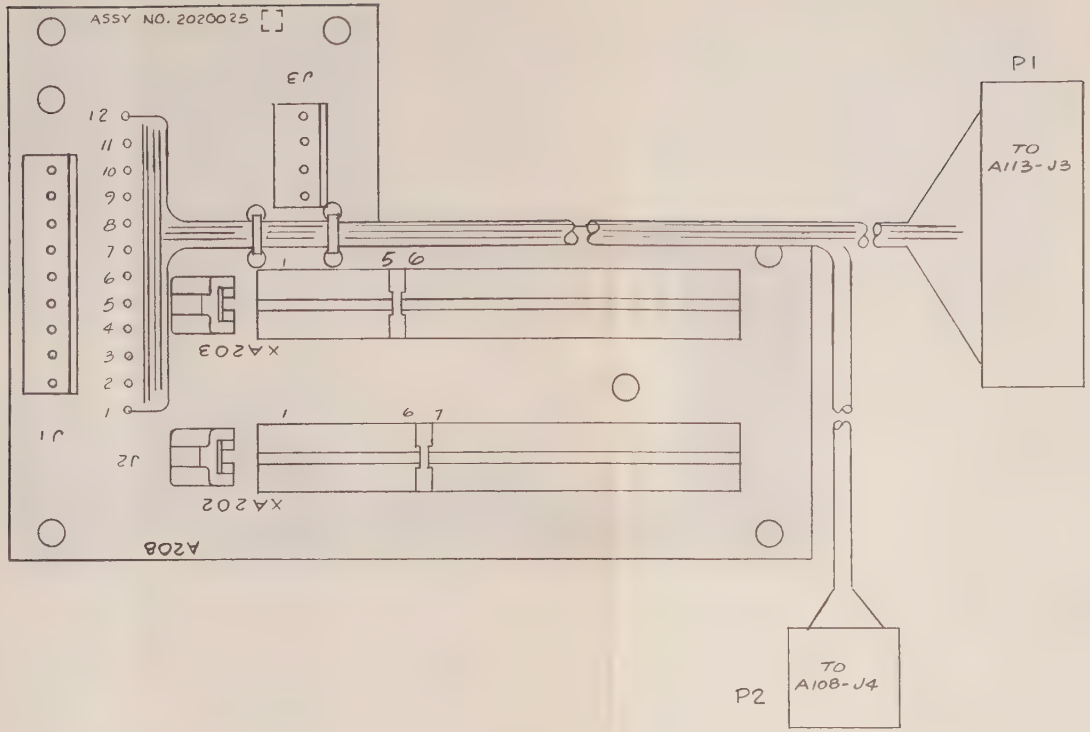


FIGURE 9-18B
SCHEMATIC DIAGRAM
VIDEO AMPLIFIER (A204)

0144M



025D

FIGURE 9-19A
COMPONENT LOCATOR
CONVERTER INTERCONNECT (A208)

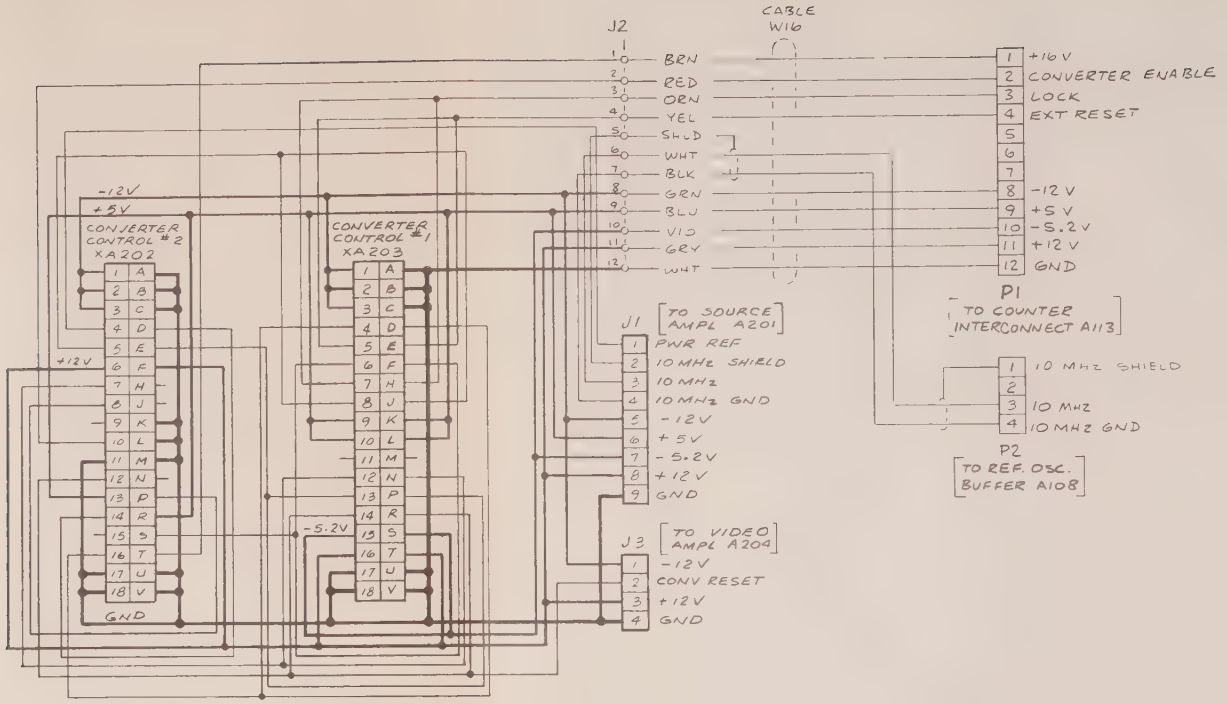


FIGURE 9-19B
SCHEMATIC DIAGRAM
CONVERTER INTERCONNECT (A208)

SECTION O

OPTIONS

O-1. This section provides descriptions, specifications (where applicable), schematic diagrams and component locators, for the options available for use with the EIP 350D/351D Autohet Frequency Counters.

OPT	DESCRIPTION
01	YIG PRESET - PROGRAMMABLE
02	YIG PRESET - THUMBWHEEL
03	OVEN STABILIZED OSCILLATOR (5×10^{-9})
04	OVEN STABILIZED OSCILLATOR (1×10^{-9})
05	OVEN STABILIZED OSCILLATOR (5×10^{-10})
06	PROGRAMMABLE OFFSETS
07	REMOTE PROGRAMMING
08	-30 dBm SENSITIVITY - BAND III
09	BCD OUTPUT
10	REAR PANEL INPUT CONNECTORS
11	BAND II DELETED
12	EXTENDED BAND III RANGE - 350D
15	AUTOMATIC INPUT LEVEL CONTROL

OPTION 01
YIG PRESET - PROGRAMMABLE

O1-1. DESCRIPTION

O1-2. This option allows the user to program the starting frequency of the sweep in Band III (825 MHz to 12.4/18 GHz). Increments of 200 MHz may be programmed by grounding the appropriate inputs using standard 1-2-4-8 BCD code. These inputs drive Converter Control 2 inverters A202U7 and U9 to preset the DCUs of DAC 1 on A202.

O1-3. For proper Converter operation, it is necessary that the sweep function not be interfered with. This requires that the minimum frequency to be measured must be at least 275 MHz above the preset frequency. It also imposes the requirement that the preset number be at least 275 MHz above any other frequencies present.

O1-4. Provided the above restrictions are met, Option 01 may be used both for the purpose of speeding acquisition time, and to measure a signal in the presence of a lower frequency signal.

J3 Pin No.	Function
16	10^8 B (200 MHz)
17	10^8 C (400 MHz)
18	10^8 D (800 MHz)
19	10^9 A (1 GHz)
20	10^9 B (2 GHz)
21	10^9 C (4 GHz)
22	10^9 D (8 GHz)
23	10^{10} A (10 GHz)
24	Ground
25	+ 5 Vdc

TABLE O1-1
J3 CONTACT GROUNDING FOR
PROGRAMMABLE YIG PRESET
OPTION 01

O1-5. OPERATION

a. Enter preset frequency into the counter with consideration for programming requirements.

b. Press **RESET** button.

EXAMPLE: To measure 8 GHz signal in presence of 4 GHz signal (both signals above minimum sensitivity of counter), program counter for 7 GHz; press **RESET** button. Counter begins sweep at 7 GHz and locks on 8 GHz signal.

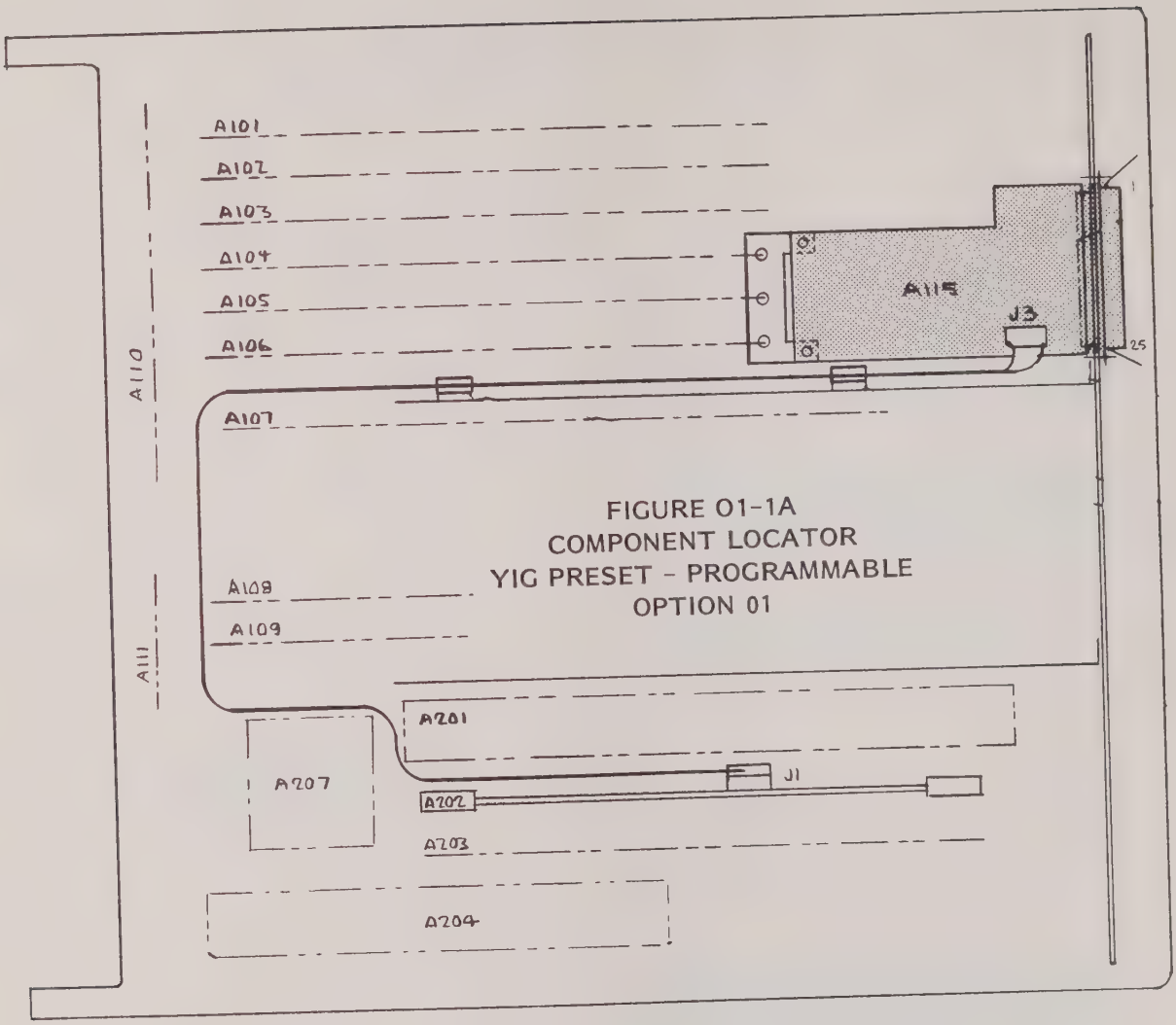
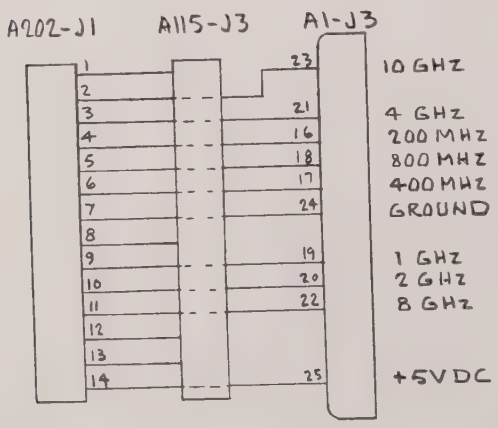


FIGURE 01-1A
COMPONENT LOCATOR
YIG PRESET - PROGRAMMABLE
OPTION 01



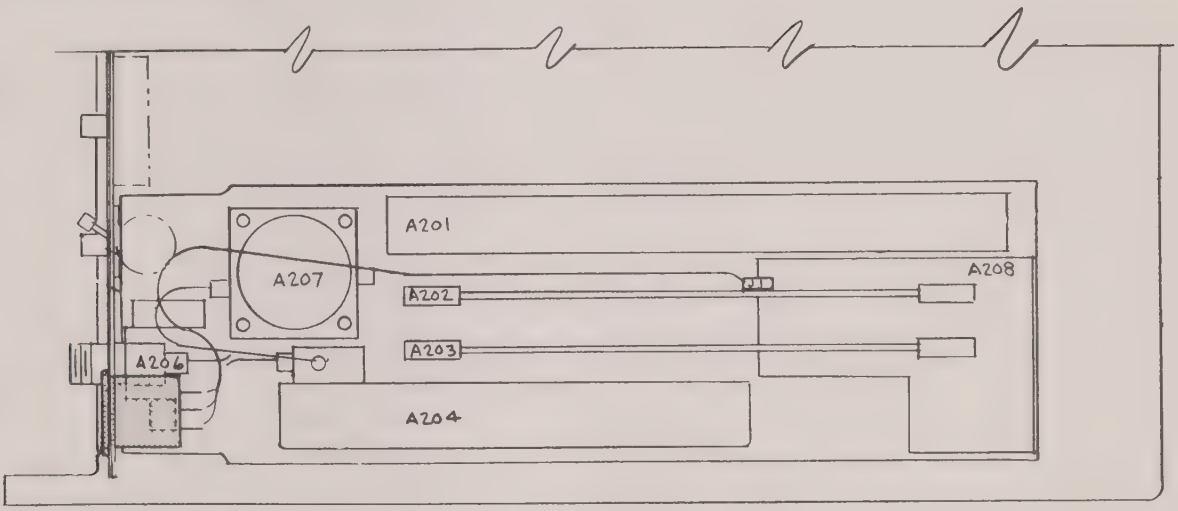
Refer to Option 07, Figure 07-1 for Component Locator and Schematic Diagram for A115 Programming Board.

FIGURE 01-1B
INTERCONNECTION DIAGRAM
YIG PRESET - PROGRAMMABLE
OPTION 01

OPTION 02
YIG PRESET - THUMBWHEEL

O2-1. DESCRIPTION

O2-2. This option is functionally identical to Option 01 with the exception that ground contact closure is provided by a 3-digit thumbwheel switch mounted on the front panel of the counter. Comb start frequency may be read directly from the switch.



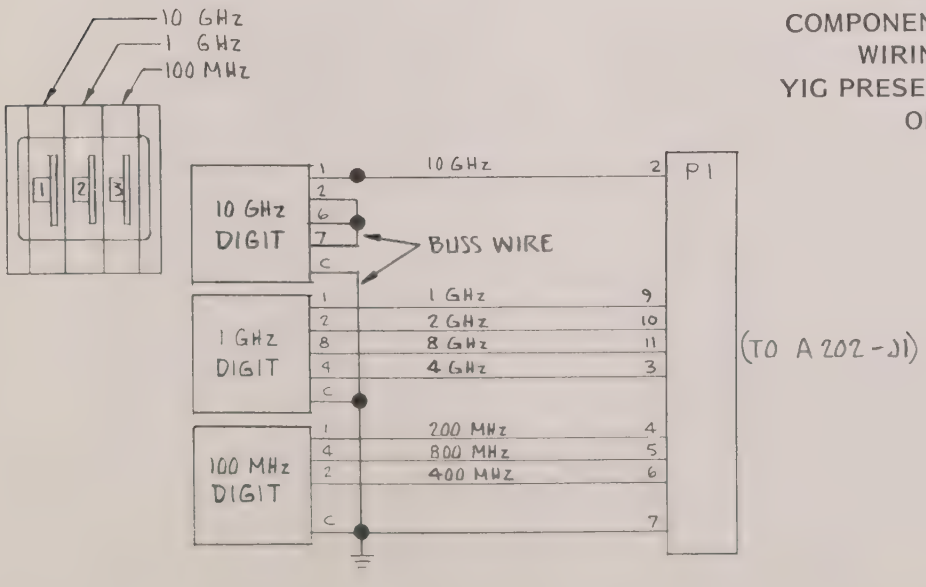


FIGURE O2-1
COMPONENT LOCATOR AND
WIRING DIAGRAM
YIG PRESET - THUMBWHEEL
OPTION 02

OPTIONS 03, 04, AND 05
HIGH STABILITY TIME BASE
(OVEN STABILIZED CRYSTAL OSCILLATOR)

O3-1. DESCRIPTION

O3-2. Three Oven Stabilized Oscillators are available as options for the 350D/351D Counters. Specifications for the three options are listed in Table O3-1. These options reduce the counter inaccuracy (see Section 6, paragraphs 6-8 through 6-26) due to both temperature and time.

O3-3. When either Option 03, 04, or 05 is installed, the TCXO (A116) is removed from the Reference Oscillator PC Board (A108), and components are added to A108 and Counter Chassis A1 (see Section 9, Figure 9-10). The added components include Oven Oscillator power transformer A114T1, 28 Vdc Oven Power Supply A114, and connector A108J3.

O3-4. The 28 volt Power Supply is on and operating as long as the counter is plugged into an active source of AC power, irrespective of the counter's **POWER** On/Off switch. Primary wiring of the oven oscillator power transformer is shown in Section 9, Figure 9-9. The balance of the circuit is conventional: full-wave bridge rectifier CR1, filter C1, regulator U1, series pass transistor Q1, protective diodes CR1-CR3, and voltage control R3.

CHARACTERISTIC	OPTION 03	OPTION 04	OPTION 05
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 1 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms		
0° to +50° C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$
±10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

TABLE O3-1
SPECIFICATIONS
OVENIZED OSCILLATOR OPTIONS

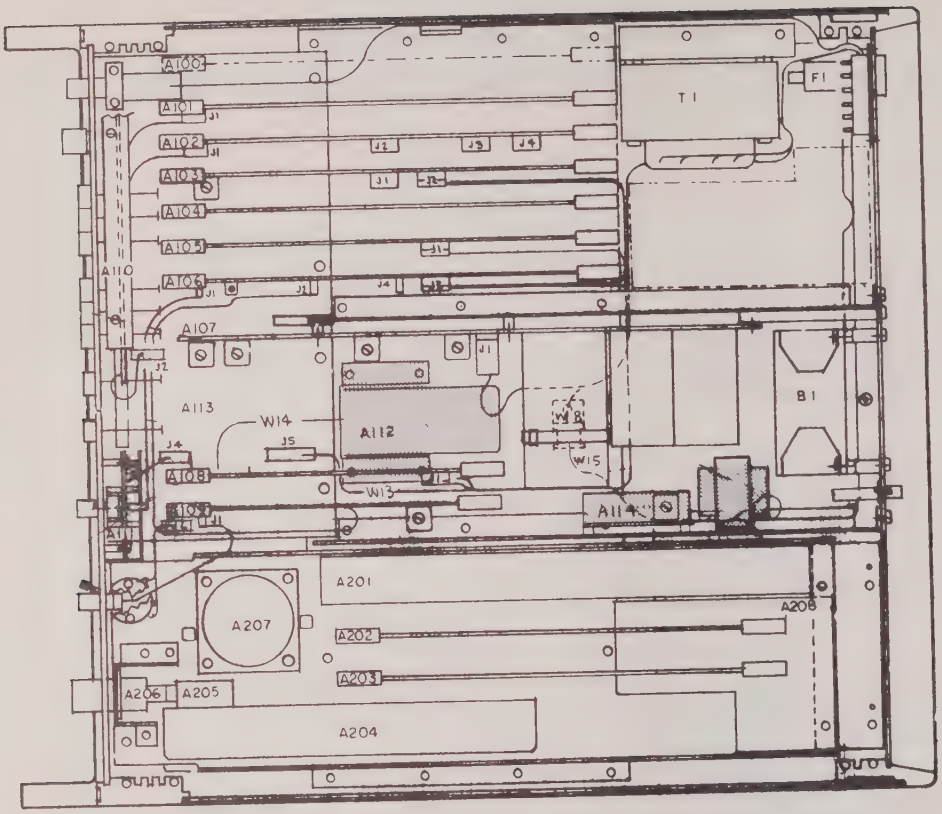
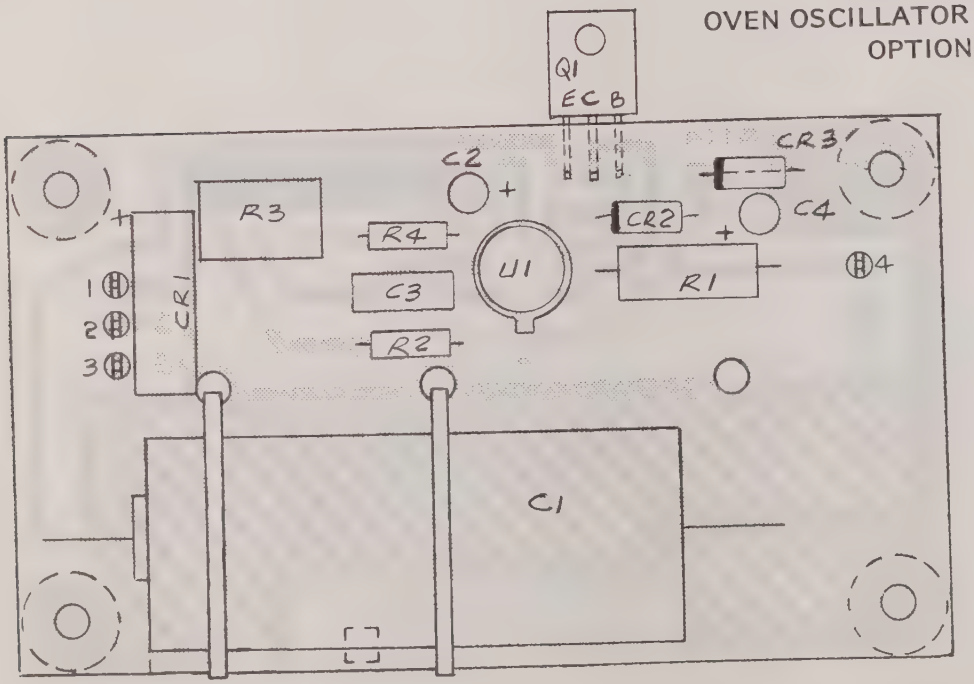


FIGURE 03-1A
COMPONENT LOCATORS
OVEN OSCILLATOR POWER SUPPLY
OPTIONS 03, 04, 05



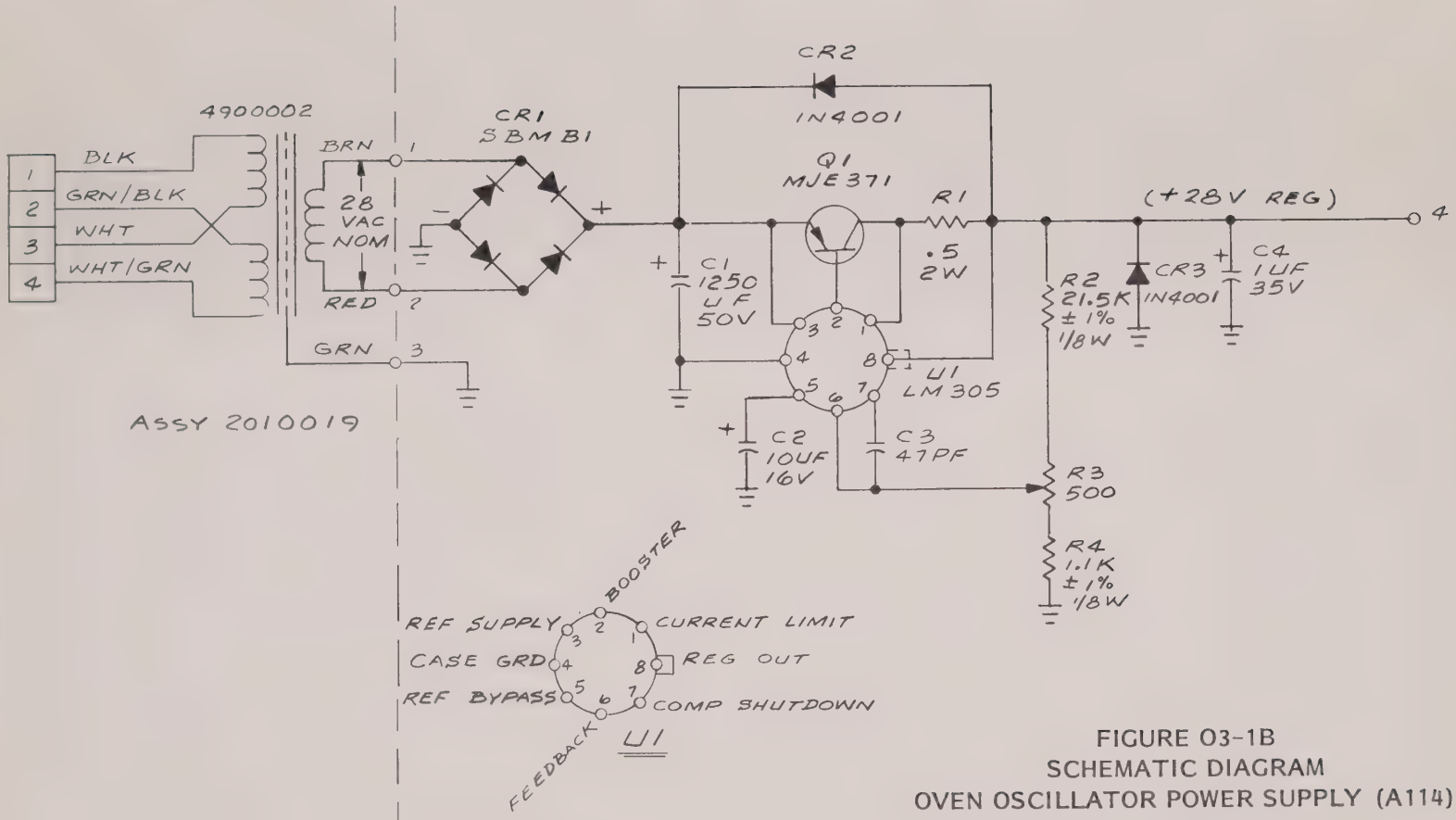


FIGURE 03-1B
SCHEMATIC DIAGRAM
OVEN OSCILLATOR POWER SUPPLY (A114)
OPTIONS 03, 04, 05

OPTION 06
PROGRAMMABLE OFFSETS

O6-1. GENERAL DESCRIPTION

O6-2. This option allows the displayed reading of any frequency to be increased or decreased by any number in 100 kHz increments.

O6-3. For positive offsets, the desired number may be programmed directly on 24 input lines (4-line BCD code on each of six digits). Activating the $\overline{\text{OFFSET ENABLE}}$ command will then cause the reading to be offset by the programmed frequency.

O6-4. Negative offsets require that the nines complement of the number be programmed and that the $\overline{\text{OFFSET MINUS}}$ command be activated. The nines complement of a number is obtained by subtracting the number from 99.9999 GHz.

O6-5. All inputs are programmed by ground contact closure or application of a TTL "0" level. Pin connections are shown in Table O6-1.

O6-6. CIRCUIT DESCRIPTION

O6-7. Circuitry required for the option is contained on two PC boards. Programming Option Board A115 contains the inverters used as buffers for the input information. Offset Control Unit A100 contains the remaining control circuitry.

O6-8. The six digit offset input is used to directly preset the six DCUs on Count Chain 2 (A102). This then requires that the 3 MSD information from the Converter (in Band III operation) must be serially added to the preset information. This is the major function of the Offset Control unit.

O6-9. The second function of the unit is to provide a single pulse to the 100 kHz DCU of A102 during negative offset.

O6-10. During $\overline{\text{SEQUENCE GENERATOR "0"}}$, 3 MSD information from the Converter is preset into U6, U7, and U8. The $\overline{\text{OFFSET LOAD}}$ command is generated (U2 pin 6) and, if $\overline{\text{OFFSET MINUS}}$ is low (negative offset), U4B is set.

O6-11. At $\overline{\text{SEQUENCE GENERATOR "1"}}$, U3A is enabled and divides the input 2.5 MHz clock to 1.25 MHz. U3B inhibits the sequence generator and enables U4A. The first clock pulse triggers U4A which activates the GATE X 100 MHz signal and operates a single ADD X 100 kHz pulse if negative offset is selected. Clock pulses then simultaneously appear at the ADD X 100 MHz output and the $\overline{\text{COUNT DOWN}}$ input to U6. Pulses continue until U6, U7, and U8 have counted down to zero. U3B is then reset, which in turn resets U4A, ends the cycle, and removes the $\overline{\text{SEQUENCE GENERATOR INHIBIT}}$.

O6-12. Programming connector type: Amphenol 57-40500, 50 pin female. Mating connector: Amphenol 57-30500, 50 pin male.

J3 Pin	Function
14	Ground
15	Offset $\overline{\text{Enable}}$
26	10^5 A (100 kHz)
27	10^5 B (200 kHz)
28	10^5 C (400 kHz)
29	10^5 D (800 kHz)
30	10^6 A (1 MHz)
31	10^6 B (2 MHz)
32	10^6 C (4 MHz)
33	10^6 D (8 MHz)
34	10^7 A (10 MHz)
35	10^7 B (20 MHz)
36	10^7 C (40 MHz)
37	10^7 D (80 MHz)
38	10^8 A (100 MHz)
39	10^8 B (200 MHz)
40	10^8 C (400 MHz)
41	10^8 D (800 MHz)
42	10^9 A (1 GHz)
43	10^9 B (2 GHz)
44	10^9 C (4 GHz)
45	10^9 D (8 GHz)
46	10^{10} A (10 GHz)
47	10^{10} B (20 GHz)
48	10^{10} C (40 GHz)
49	10^{10} D (80 GHz)
50	Offset Plus/$\overline{\text{Minus}}$

TABLE O6-1
J3 CONTACT GROUNDING FOR
PROGRAMMABLE OFFSET
OPTION 06

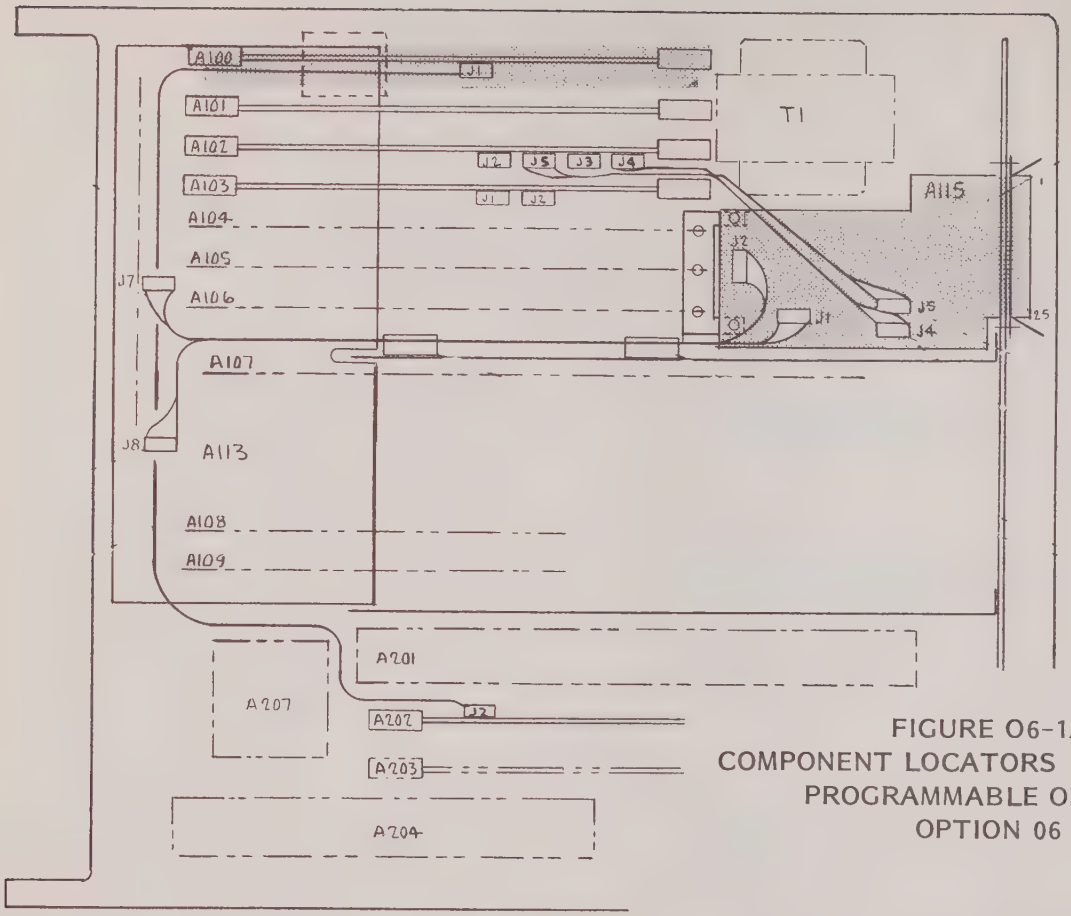
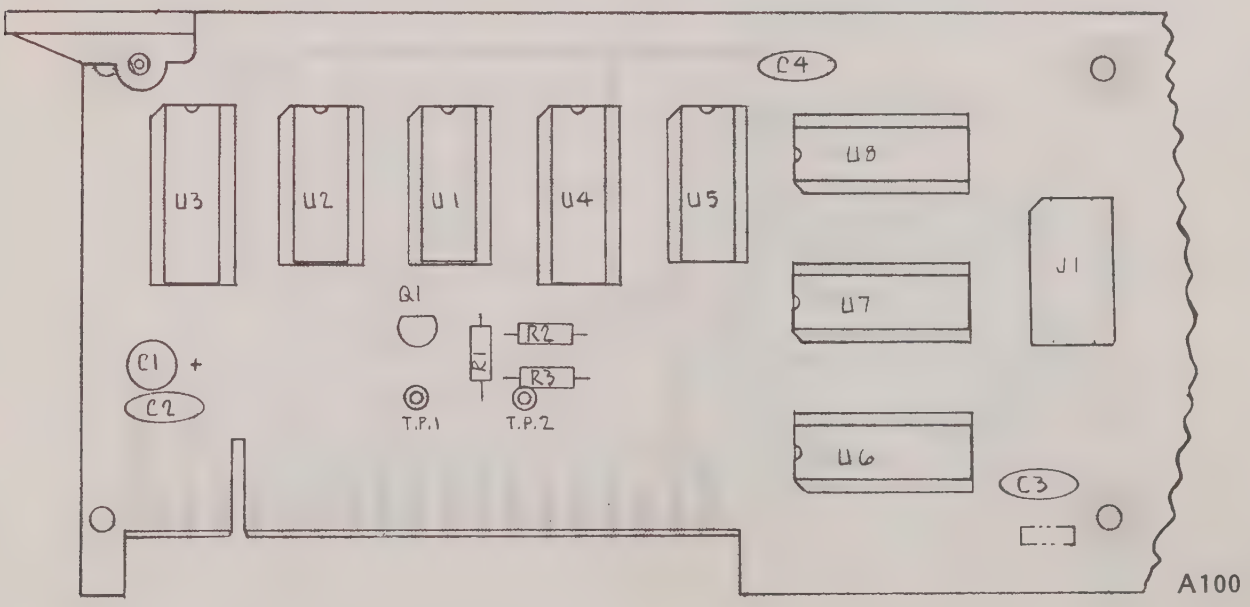


FIGURE O6-1A
COMPONENT LOCATORS (A100 & A115)
PROGRAMMABLE OFFSETS
OPTION 06

Refer to Option 07, Figure O7-1 for Component Locator and Schematic Diagram for A115 Programming Board.



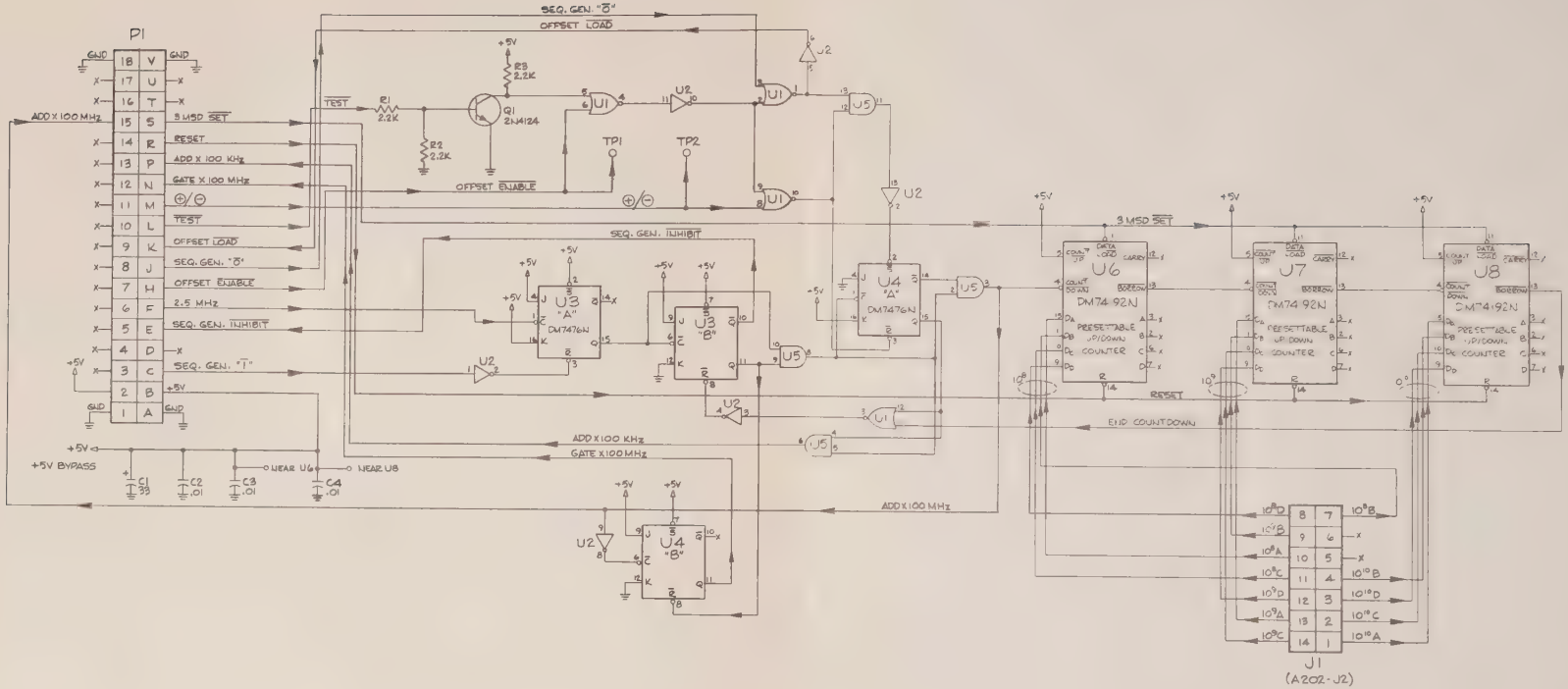


FIGURE 06-1B
SCHEMATIC DIAGRAM
PROGRAMMABLE OFFSETS
OPTION 06

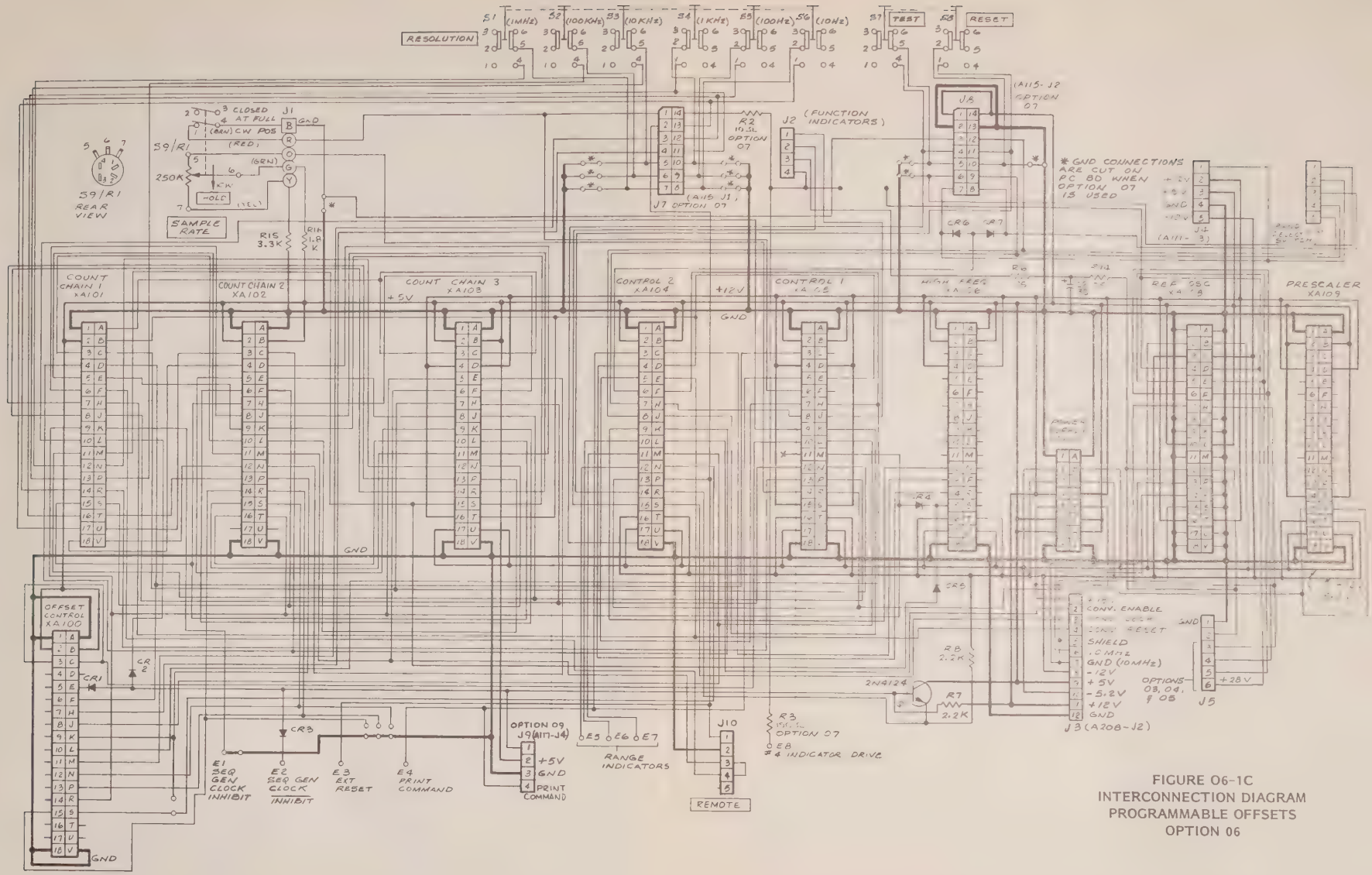


FIGURE 06-1C
INTERCONNECTION DIAGRAM
PROGRAMMABLE OFFSETS
OPTION 06

OPTION 07
REMOTE PROGRAMMING

O7-1. GENERAL DESCRIPTION

O7-2. Most of the functions which are normally controlled from the front panel of the counter may be remotely programmed by this option. These functions are:

a. $\overline{\text{10 Hz RESOLUTION}}$
b. $\overline{\text{100 Hz RESOLUTION}}$
c. $\overline{\text{1 kHz RESOLUTION}}$
d. $\overline{\text{HOLD}}$
e. $\overline{\text{RESET}}$
f. $\overline{\text{TEST}}$
g. $\overline{\text{BAND I SELECT}}$
h. $\overline{\text{BAND II SELECT}}$
i. $\overline{\text{BAND III SELECT}}$

O7-3. In addition to the front panel controls, an additional command $\overline{\text{COUNTER RESET}}$ is also available. This command resets the counter and initiates a new reading without resetting the Converter.

O7-4. The LOCAL/$\overline{\text{REMOTE}}$ input activates the remote functions. This and all remote commands are activated by ground contact closure or a TTL "0" level. Pin connections to the rear panel are shown in Table O7-1.

O7-5. CIRCUIT DESCRIPTION

O7-6. In the standard instrument, all front panel control switches are returned to ground through removable links on the counter Interconnect Board (A110). These are cut when the Remote Programming option is installed. The switch returns are then grounded by the added program circuits in the LOCAL mode. Grounding the LOCAL/$\overline{\text{REMOTE}}$ input then disables the front panel switches. The opposite contacts of each switch are then driven by the remote control circuitry.

O7-7. The circuits which ground the front panel switch returns are open-collector inverters driven in common by the LOCAL/$\overline{\text{REMOTE}}$ input signal. The drivers in parallel with the opposite contacts of the switches are also open-collectors, each driven by a NOR gate. One input to each NOR gate is the LOCAL/$\overline{\text{REMOTE}}$ control, which opens all inverters in the high (LOCAL) state. In $\overline{\text{REMOTE}}$ the other NOR inputs (driven by the rear panel inputs) are in control.

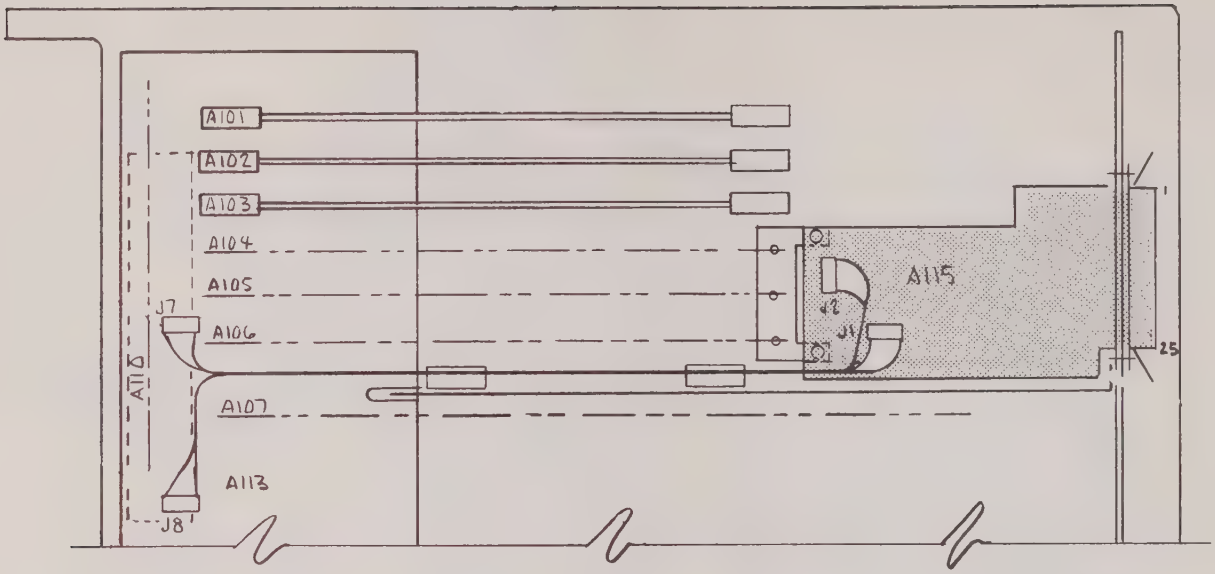
O7-8. If the $\overline{\text{HOLD}}$ is not energized, front panel sample rate determines cycle time. In remote operation, however, the front panel **HOLD** is ineffective.

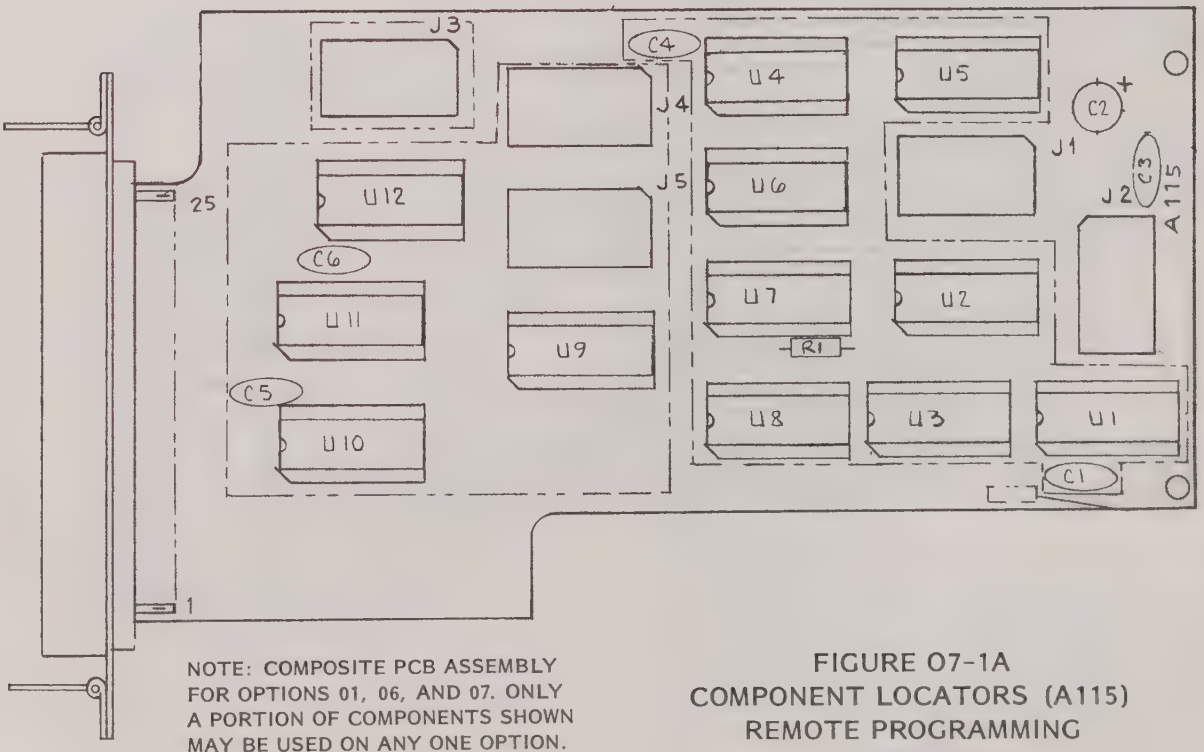
O7-9. If none of the **RESOLUTION** switches are grounded, the counter will operate with a one second gate.

O7-10. Programming connector type: Amphenol 57-40500, 50 pin female. Mating connector: Amphenol 57-30500, 50 pin male.

J3 Pin No.	Function
1	No Connection
2	1 kHz Resolution
3	100 Hz Resolution
4	$\overline{\text{Hold}}$
5	$\overline{\text{Reset}}$
6	$\overline{\text{Test}}$
7	Counter Reset
8	10 Hz Resolution
9	$\overline{\text{Band I, Lo-Z}}$
10	$\overline{\text{Band I, Hi-Z}}$
11	$\overline{\text{Band II}}$
12	$\overline{\text{Band III}}$
13	Local/$\overline{\text{Remote}}$
14	Ground

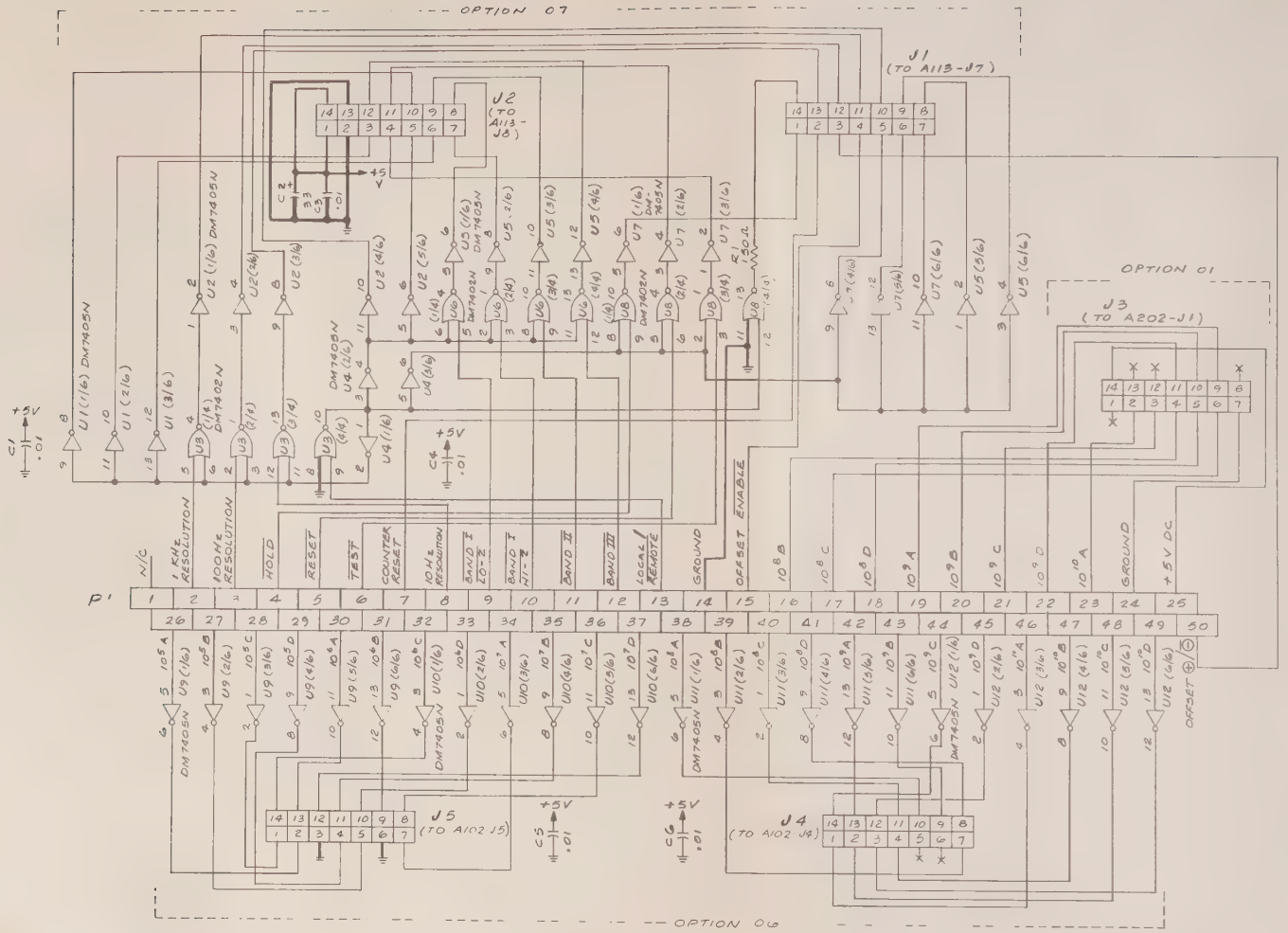
TABLE O7-1
J3 CONTACT GROUNDING FOR
REMOTE PROGRAMMING
OPTION 07





NOTE: COMPOSITE PCB ASSEMBLY FOR OPTIONS 01, 06, AND 07. ONLY A PORTION OF COMPONENTS SHOWN MAY BE USED ON ANY ONE OPTION.

FIGURE 07-1A
COMPONENT LOCATORS (A115)
REMOTE PROGRAMMING
OPTION 07



NOT USED
U1	4|6, 5|6, 6|6
U2	6|6
U4	4|6, 5|6, 6|6

U1 THRU U12:
PIN # 7 = GND
PIN # 14 = +5V

FIGURE 07-1B
SCHEMATIC DIAGRAM (A115)
REMOTE PROGRAMMING
OPTION 07

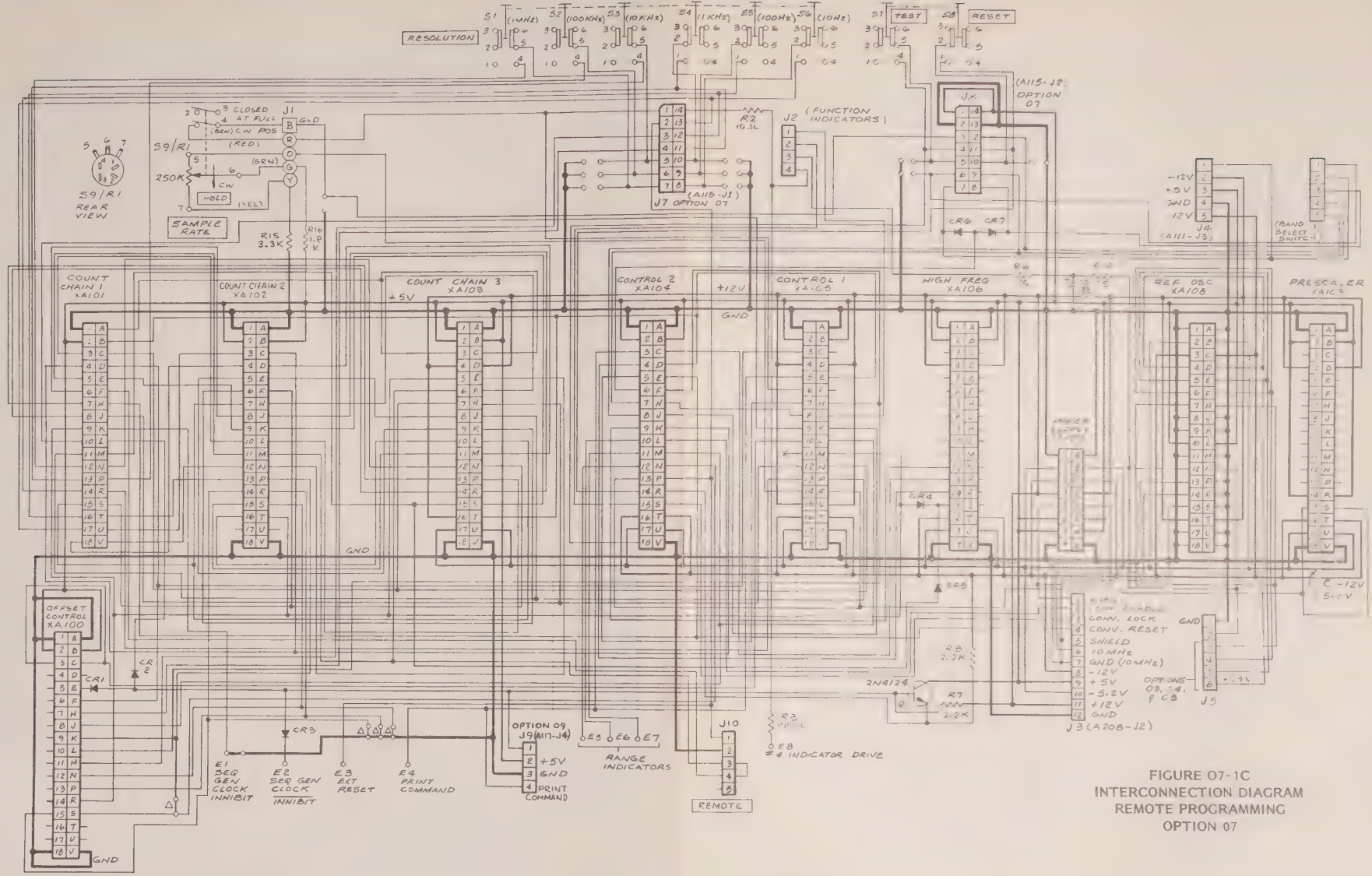


FIGURE 07-1C
INTERCONNECTION DIAGRAM
REMOTE PROGRAMMING
OPTION 07

OPTION 08
BAND III SENSITIVITY INCREASE

O8-1. DESCRIPTION

O8-2. Through factory selected components, Band III sensitivity between 1.1 GHz and 6.5 GHz is increased to -30 dBm. Complete Band III Specifications for this option are given in Table O8-1.

OPTION O8

Band III Minimum Sensitivity:

825 MHz to 1.1 GHz:	-20 dBm (18 mV rms)
1.1 GHz to 6.5 GHz:	-30 dBm (7 mV rms)
6.5 GHz to 12.4 GHz:	-25 dBm (22 mV rms)
12.4 GHz to 18.0 GHz:	-20 dBm (18 mV rms)*

* 351D only.

Table O8-1
Band III Sensitivity

OPTION 09
BCD OUTPUT

O9-1. DESCRIPTION

O9-2. This assembly provides binary coded decimal outputs to the rear panel of the counter corresponding to the applied input frequency. A $\overline{\text{PRINT}}$ command indicates the presence of valid data, while an INHIBIT input is available to allow the user to prevent the information from being altered. Refer to Table O9-2 for rear panel connections.

O9-3. Each output line from the latches associated with the counting chain (A102, A103) then feeds through an inverter to the rear panel Digital Output Connector J2.

O9-4. A positive INHIBIT level (+2 to +50 V) turns on Q1. This in turn, generates a $\overline{\text{SEQUENCE INHIBIT}}$ command to prevent the counter from continuing its sequence. This command allows the user to prevent stored information from being altered.

BCD Code	1 - 2 - 4 - 8
Format	11 data digits in parallel form
"0" State Level	0 to 0.4 V, 5 mA current sink capability
"1" State Level	+5 V, 2kohm source impedance
Negative Ref	Ground
Positive Ref	+5 V, 22 ohm source impedance
Print Command	+5 V to 0 V step, fall time 1 microsecond 20 microsecond width. 2kohm source impedance.
Hold Off Requirement	Maximum: 50 V; minimum: 2 V.

TABLE O9-1
SPECIFICATIONS

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	10^1 A	18	10^9 B	34	10^5 C
2	10^1 B	19	10^{10} A	35	10^5 D
3	10^2 A	20	10^{10} B	36	10^6 C
4	10^2 B	21	10^0 A	37	10^6 D
5	10^3 A	22	Inhibit	38	10^7 C
6	10^3 B	23	10^0 B	39	10^7 D
7	10^4 A	24	- Ref	40	10^8 C
8	10^4 B	25	+ Ref	41	10^8 D
9	10^5 A	26	10^1 C	42	10^9 C
10	10^5 B	27	10^1 D	43	10^9 D
11	10^6 A	28	10^2 C	44	10^{10} C
12	10^6 B	29	10^2 D	45	10^{10} D
13	10^7 A	30	10^3 C	46	10^0 C
14	10^7 B	31	10^3 D	47	10^0 D
15	10^8 A	32	10^4 C	48	Print Command
16	10^8 B	33	10^4 D	49	No Connection
17	10^9 A			50	Ground

NOTE: The 10^0 bit is the least significant digit, and corresponds to the 1 Hz output. A, B, C, and D, are the 1, 2, 4, and 8, bits of each binary coded decimal output digit.

TABLE 09-2
J2 CONTACT GROUNDING FOR
BCD DIGITAL OUTPUT
OPTION 09

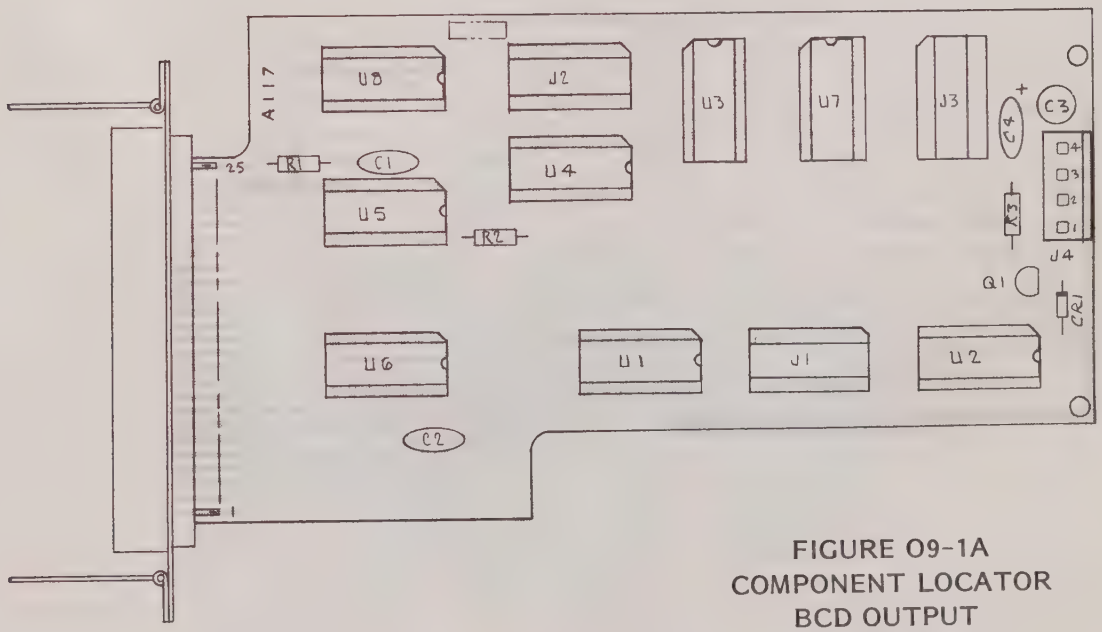
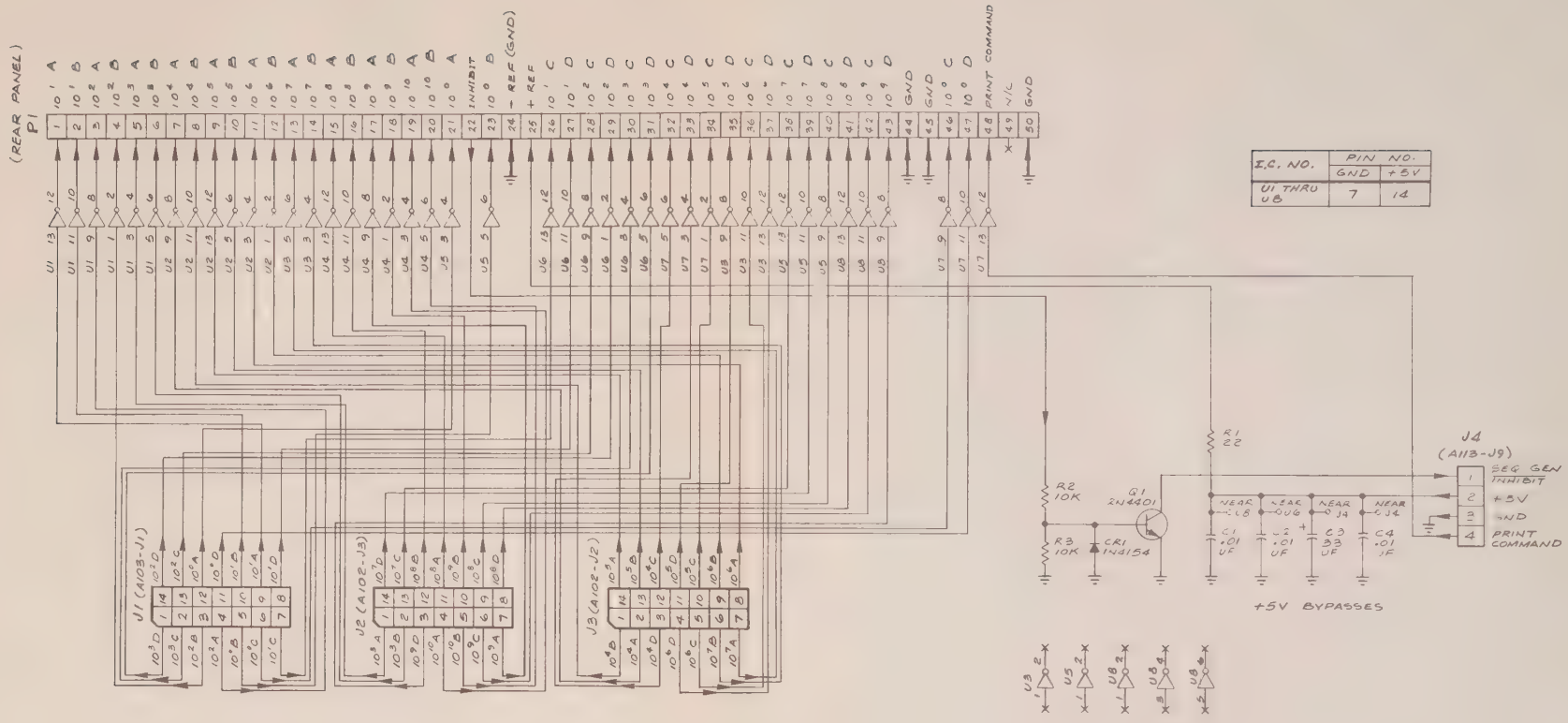


FIGURE 09-1A
COMPONENT LOCATOR
BCD OUTPUT
OPTION 09



I.C. NO.	PIN NO.	
	GND	+5V
U1 THRU U8	7	14

FIGURE 09-1B
SCHEMATIC DIAGRAM
BCD OUTPUT
OPTION 09

OPTION 10
REAR PANEL INPUTS

O10-1. DESCRIPTION

O10-2. Band I input connector and Preamplifier (A111), and Band II input connector, moved to rear panel. Converter assembly is reversed end-for-end, to place the Band III input connector at rear panel. All specifications remain as stated for front panel connectors.

OPTION 11
BAND II DELETED

O11-1. DESCRIPTION

O11-2. Band II input connector and Prescaler (A109) removed. Delete all manual references to Band II operation and components.

OPTION 12
350D BAND III FREQUENCY RANGE EXTENDED

O12-1. DESCRIPTION

O12-2. Band III frequency range of 350D extended through use of factory selected components to 825 MHz to 13.5 GHz. Sensitivity between 12.4 GHz and 13.5 GHz is -20 dBm (22 mV rms). All other specifications remain as stated in the manual.

OPTION 15

AUTOMATIC INPUT LEVEL CONTROL

O15-1. GENERAL

O15-2. Option 15 provides a closed loop leveling system at the input to the counter which maintains a relatively constant input level to the Mixer (approx. -20 dBm). This results in an improvement in the burnout level (+30 dBm compared to +20 dBm of a standard unit), and an increase in the operating signal level. Typically, operation up to +20 dBm is possible. In addition, Option 15 provides improved measurement capability in the presence of spurious signals and wideband noise. Refer to Table O15-1 for specifications pertinent to this option.

O15-3. OPERATION

O15-4. A functional block diagram of the Automatic Level Control System is shown in Figure O15-1. Input RF power is detected in the Mixer (A205), producing a current proportional to the input power. When this current exceeds a value determined by the threshold circuit, the PIN driver is turned on, thus increasing the insertion loss through the PIN Diode Attenuator (A206).

O15-5. The PIN Diode Attenuator contains series and shunt diodes, arranged in such a manner that when appropriate currents are applied, insertion loss can be varied while both input and output ports maintain a nominal 50Ω impedance. The PIN Driver contains appropriate shaping networks to supply the correct currents at all attenuation levels.

Maximum input level (burnout):	+30 dBm (1 W)
Maximum operating level (typ):	+20 dBm (100 mW)
Dynamic operating range (typ):	Approx 45 db

TABLE O15-1
SPECIFICATIONS
OPTION 15

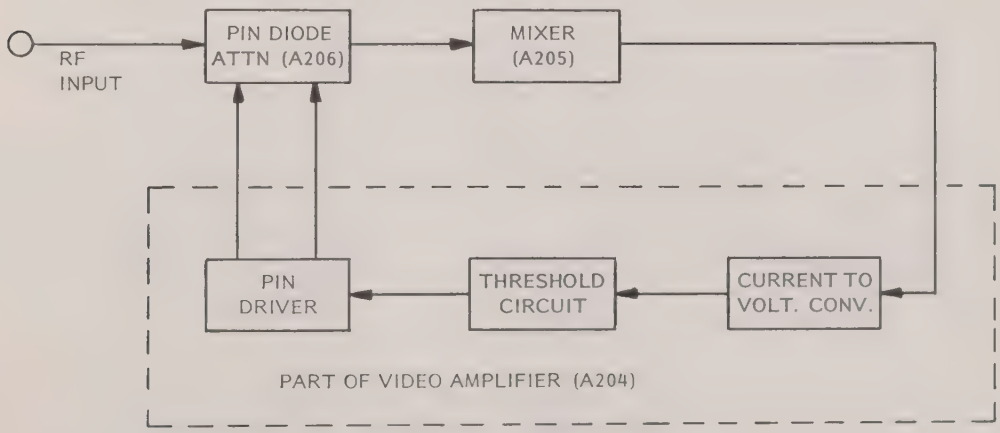


FIGURE O15-1
BLOCK DIAGRAM
AUTOMATIC LEVEL CONTROL SYSTEM
OPTION 15

O15-6. ADJUSTMENTS

NOTE: Incorporation of Option 15 into a 350D/351D or 331 Counter, requires that paragraph 6-7d be replaced by the following adjustment procedure:

d. Preliminary Comb Leveling, Bias, and Threshold:

(1) Set Bias Adjust (A201R16) fully counter-clockwise.

(2) Connect dual trace oscilloscope as follows:

Ch.A	A204TP1 (Mixer Detected output)
Ch. B	A201FL1 (Power Level input)
Ext. Trig.	A203TP8 (CONV. RESET)

(3) Set Channel A for AC coupling, 20 mV/cm. Set Channel B for DC coupling, 2 V/cm.

(4) Terminate Band III input connector in 50 ohms; a 6 dB (or greater) pad is adequate.

(5) Adjust potentiometers on A202 so the maximum comb line amplitude does not appreciably vary from the levels shown in Table O15-2.

(6) If necessary, readjust A202R16 slightly for optimum flatness. This adjustment may necessitate repeating step (5).

(7) Remove the 6 dB terminating pad from the Band III input connector.

(8) Unplug Source/Amplifier power plug A208J1 (at rear of Counter Interconnect PCB A208).

(9) Connect a 3 dB pad to the Band III input connector. Apply a +3 dBm signal at 1.0 GHz to pad.

(10) Square-wave modulate the 1.0 GHz signal. Observe square-wave signal at A204TP1.

(11) Adjust A204R61 until square-wave at A204TP1 is 90 to 100 mV in amplitude.

(12) Reconnect Source/Amplifier power plug.

ADJUST-MENT	COMB LINE AFFECTED (GHz)	NOMINAL MAXIMUM LEVEL 350D	351D
A202R95	1.0, 1.2	60 mV	60 mV
A202R97	1.4, 1.6, 1.8	60 mV	60 mV
A202R93	2.0, 2.2, 2.4, 2.6, 2.8	60 mV	60 mV
A202R91	3.0, 3.2, 3.4, 3.6, 3.8	60 mV	60 mV
A202R89	4.0, 4.2, 4.4, 4.6, 4.8	60 mV	60 mV
A202R87	5.0, 5.2, 5.4, 5.6, 5.8	60 mV	60 mv
A202R85	6.0, 6.2, 6.4, 6.6, 6.8	60 mV ±	60 mV
A202R83	7.0, 7.2, 7.4, 7.6, 7.8	No Max	60 mV
A202R82*	8.0, 8.2, 8.4, 8.6, 8.8	No Max	60 mV
A202R80*	9.0, 9.2, 9.4, 9.6, 9.8	No Max	60 mv ¤

* Selected at Test ± 6.0 and 6.2 only ¤ 9.0 GHz only

TABLE O15-2
COMB LEVEL ADJUSTMENTS
PIN DRIVER/VIDEO AMPLIFIER
OPTION 15

TABLE O15-3. PARTS LIST

OPTION 15 - AUTOMATIC LEVEL CONTROL

A204/A205/A206 - ASSY 2010061 (SEE NOTE)

A204 PCB PARTS:

REF	SAME	EIP P/N	DESCRIPTION
C1		2250018	C: MICA 470 PF
C2		2150003	C: CER .01 UF
C3		2160002	C: CER 1.0 PF
C4	C2		
C5		2250006	C: MICA 180 PF
C6-9	C2		
C10	C5		
C11-14	C2		
C15	C5		
C16-19	C2		
C20-21		2250009	C: MICA 200 PF
C22	C2		
C23		2150001	C: CER .001 UF
C24-25	C2		
C26			NOT USED
C27	C23		
C28-30	C2		
C31	C5		
C32-35	C2		
C36	C5		
C37-40	C2		
C41	C5		
C42-45	C2		
C46	C5		
C47		2160004	C: CER 10 PF
C48	C2		
C49		2300010	C: TANT 10 UF
C50			NOT USED
C51		2160007	C: CER 18 PF
C52	C2		
C53			NOT USED
C54-55	C2		
C56	C5		
C57-64	C2		
C65	C20		
C66		2250002	C: MICA 100 PF
C67	C2		
C68	C49		
C69	C2		
C70	C66		
CR1-2		2710022	DI: PIN
CR3-4		2710004	DI. HOT CARR
CR5			NOT USED
CR6	CR3		
CR7		2704370	DI: ZENER
CR8		2704001	DI: RECT
CR9		2704154	DI: GP
FL1			NOT USED
FL2-4		2350017	C: FDTH
J1		2610017	CONN: PLUG
J2-5		2610010	CONN: JK

REF	SAME	EIP P/N	DESCRIPTION
L1		3510005	IND: 2.2 UH
L2		3510001	IND: 0.1 UH
L3-9			PART OF PCB
L10		3510007	IND: 0.33 UH
L11-20			PART OF PCB
Q1 3		4710011	XSTR: SELECT
Q4-5		4710012	XSTR: SELECT
Q6-7	Q1		
Q8	Q4		
Q9		4710013	XSTR: SELECT
Q10 11		4704124	XSTR: NPN GP
Q12-13		4704126	XSTR: PNP GP
Q14	Q10		
Q15	Q12		
Q16	Q1		
R1		4130132	R: MET OX 1.3K
R2		4130201	R: MET OX 200
R3		4130621	R: MET OX 620
R4		4130242	R: MET OX 2.4K
R5		4130560	R: MET OX 56
R6		4120008	R: CBN FLM 8.2
R7		4130911	R: MET OX 910
R8		4010222	R: COMP 2.2K
R9		4130200	R: MET OX 20
R10	R3		
R11	R4		
R12	R5		
R13	R6		
R14	R7		
R15	R9		
R16	R3		
R17	R4		
R18	R5		
R19		4130100	R. MET OX 10
R20	R7		
R21		4010511	R: COMP 510
R22	R9		
R23	R3		
R24		4130510	R: MET OX 51
R25	R3		
R26		4010112	R: COMP 1.1K
R27		4130121	R: MET OX 120
R28		4010221	R: COMP 220
R29		4120004	R: CBN FLM 5.6
R30	R27		
R31	R4		
R32	R29		
R33	R7		
R34	R6		
R35	R9		
R36	R3		
R37	R4		
R38	R5		
R39	R6		
R40	R7		
R41		4010102	R: COMP 1K
R42	R9		
R43	R3		
R44	R4		
R45	R5		
R46	R7		
R47	R19		

REF	SAME	EIP P/N	DESCRIPTION
R48	R9		
R49	R3		
R50	R4		
R51	R5		
R52		4130821	R: MET OX 820
R53		4010xxx	R: COMP S.A.T.
R54	R19		
R55	R24		
R56		4130471	R: MET OX 470
R57		4010121	R: COMP 120
R58	R24		
R59		4130152	R: MET OX 1.5K
R60		4130272	R: MET OX 2.7K
R61		4250008	R: VAR 100K
R62		4130133	R: MET OX 13K
R63		4130103	R: MET OX 10K
R64		4130391	R: MET OX 390
R65-66	R41		
R67		4010473	R: COMP 47K
R68	R61		
R69-70		4010822	R: COMP 8.2K
R71		4010103	R: COMP 10K
R72-73		4010163	R: COMP 16K
R74	R41		
R75		4130122	R: MET OX 1.2K
R76	R63		
R77		4130910	R: MET OX 91
R78		4130163	R: MET OX 16K
R79	R1		
R80		4130222	R. MET OX 2.2K
R81-82	R63		
R83		4130102	R: MET OX 1K
R84	R52		
R85		4250003	R: VAR 1K
R86		4130681	R: MET OX
R87	R71		
R88		4068661	R: MT FLM 8.66K
R89		4130912	R: MET OX 9.1K
R90		4010471	R: COMP 470
R91		4130392	R: MET OX 3.9K
R92-95		4010240	R: COMP 24
R96	R90		
R97		4130123	R: MET OX 12K
R98		4130101	R: MET OX 100
R99		4010680	R: COMP 68
R100	R91		
R101	R67		
R102		4130472	R: MET OX 4.7K
R103		4130113	R: MET OX 11K
R104-105	R8		
R106		4130151	R: MET OX 150
R107		4130662	R: MET OX 6.2K
R108		4130303	R: MET OX 30K
R109		4010224	R: COMP 220K
U1		3040001	IC: OP AMPL
U2-4		3040741	IC: OP AMPL
U5		3041741	IC: OP AMPL

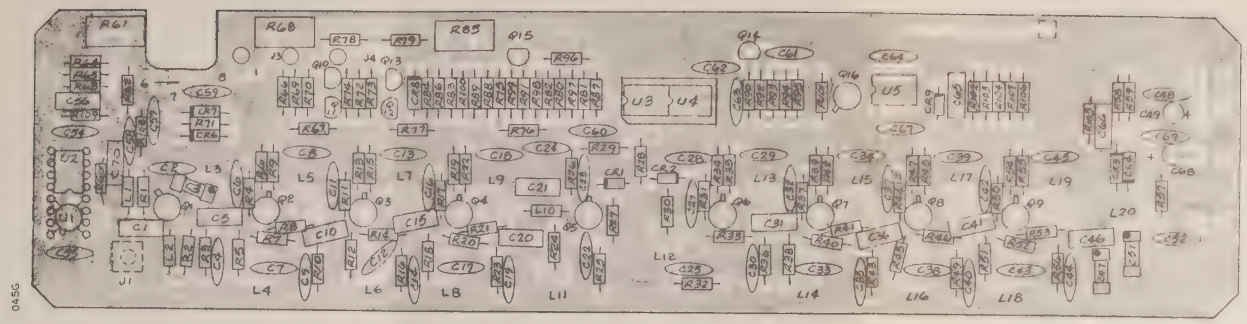
A205 PART OF ASSY 2010061

A206 PART OF ASSY 2010061

O15-7. PARTS LIST

NOTE: Mixer A205 and Attenuator A206 are factory matched to PIN Driver/Video Amplifier A204, and must be replaced as a matched set (EIP P/N: 2010061); refer to manual paragraph 5-9. Consult factory or EIP Regional Sales Representative for details of the EIP Assembly Exchange Program relating to service or replacement of any of the above noted assemblies.

PARTS LIST
FOR OPTION 15



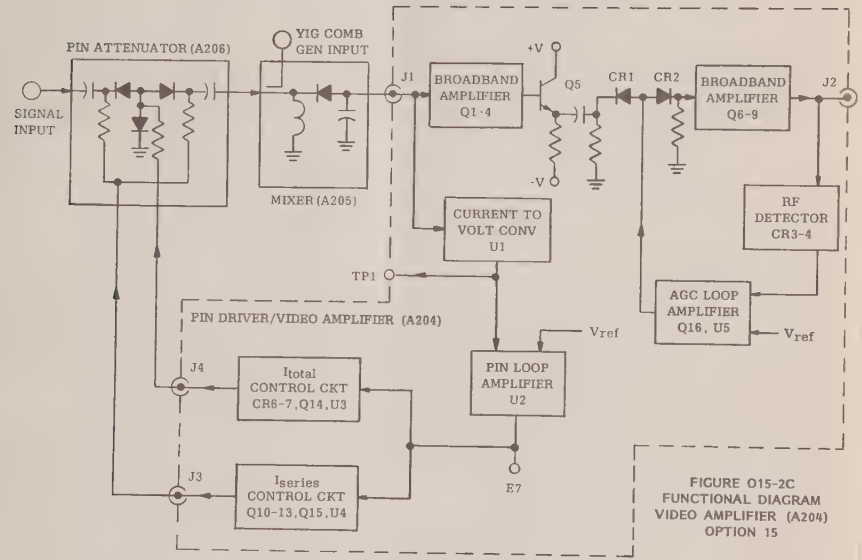


FIGURE O15-2C
FUNCTIONAL DIAGRAM
VIDEO AMPLIFIER (A204)
OPTION 15

PIN DRIVER/VIDEO AMPLIFIER (A204)

Refer to Functional Diagram — Figure O15-2C.

The PIN Driver/Video Amplifier module (A204) consists of two distinct sections: the PIN Diode Attenuator Control Loop, and the Video Amplifier.

Components of the PIN Driver include:

a. PIN Diode Attenuator (A206).
b Mixer (A205).
c. Current-to-Voltage Converter (A204U1).
d Loop Amplifier (A204U2).
e. I_{series} Control Circuit (A204Q10-13,Q15,U4).
f. I_{total} Control Circuit (A204CR6,CR7, Q14,U3).

Components of the Video Amplifier include:

a. Four-stage Broadband Amplifier (A204Q1-4).
b. PIN Attenuator Section (A204CR1, CR2,Q5).
c. Four-stage Broadband Amplifier (A204Q6-9).
d. RF Detector (A204CR3, CR4).
e. AGC Loop Amplifier (A204Q16,U5).

The PIN Diode Attenuator Control section is a simple feedback loop. DC current from the Mixer diode is converted to a voltage by U1. This voltage is compared to reference voltage (V_{ref}) at the input of U2. The difference in the two voltages is amplified by U2, and appears at E7. This voltage causes the proper currents to flow from the current generators: I_{series} and I_{total}. These currents determine the magnitude of signal attenuation in the PIN Diode Attenuator (A206).

The I_{series} and I_{total} current generators contain shaping networks that control the ratio of the currents through the series and shunt diodes in the attenuator to provide a fairly constant 50 ohm terminal impedance.

The current shaping network for I_{total} consists of CR6, CR7, R68, and R71. CR6 and CR7 produce an approximately exponential curve, while R68 and R71 produce a linear curve. Their sum determines the shape of the current into the summing node at R75.

In operation, an increase in signal power at the attenuator input results in an increase in the magnitude of DC current from the Mixer diode. The increased current causes the outputs from U1 and U2 to tend positive, increasing I_{total} while decreasing I_{series}. This produces an increase in the current through the shunt diode, and a decrease in the current through the series diodes, in a ratio which maintains a 50 ohm terminal impedance. This action decreases the magnitude of change in signal power which appears at the Mixer diode.

The Video Amplifier section amplifies the difference frequency produced by the Mixer, and applies it to Converter Control 1 (A203).

The circuit consists of eight essentially identical gain blocks and an automatic gain control. Overall gain of the Video Amplifier is nominally 56 dB, with a frequency range of 25 MHz to 275 MHz.

A typical gain block includes a single broadband transistor amplifier stabilized by series and shunt feedback, and an output matching inductor.

The AGC portion of the amplifier consists of RF level detector CR3 and CR4, loop amplifier U5, PIN Diode current driver Q16, emitter follower Q5, and PIN Attenuator diodes CR1 and CR2. The reference voltage in the AGC loop sets the maximum output power level for the Video Amplifier at 0 to +1 dBm.

FIGURE O15-2A
COMPONENT LOCATOR
VIDEO AMPLIFIER (A204)
OPTION 15

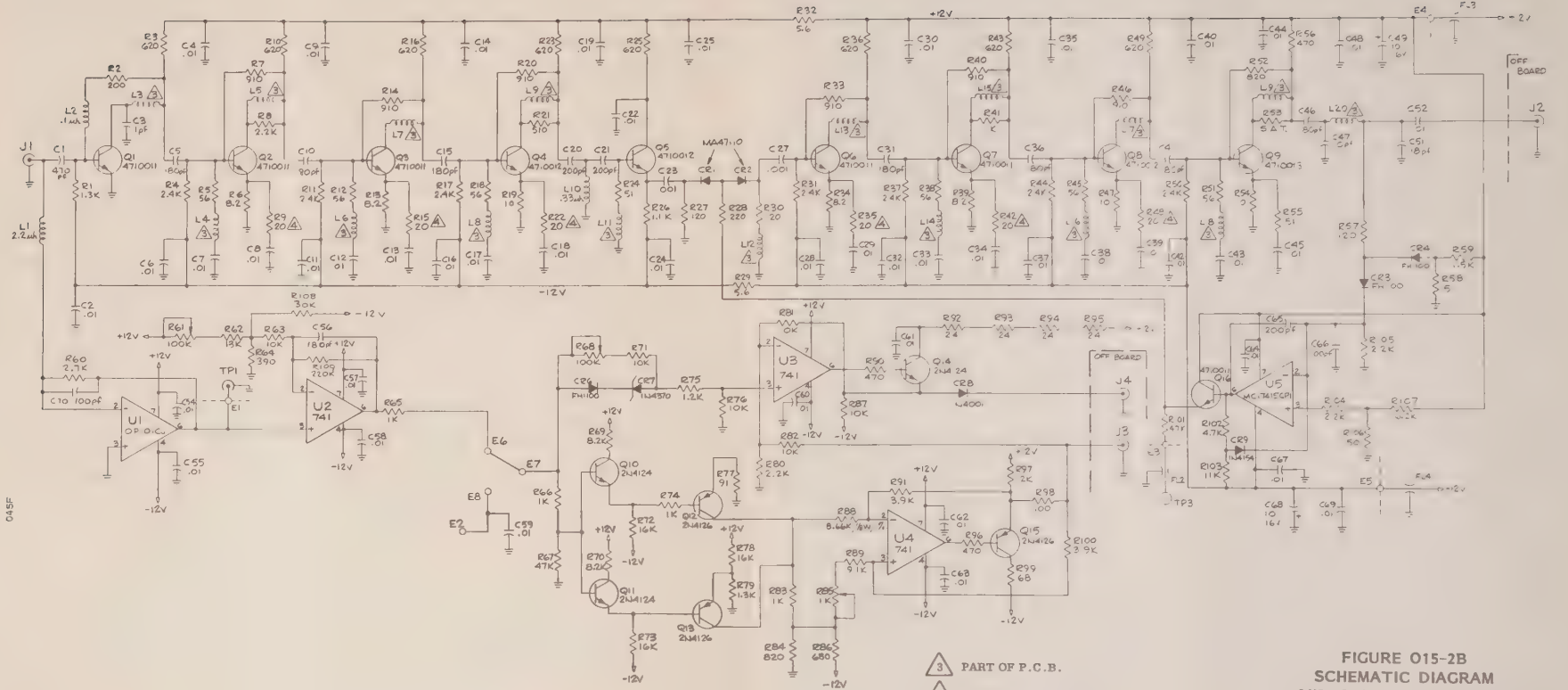


FIGURE 015-2B
SCHEMATIC DIAGRAM
VIDEO AMPLIFIER (A204)
OPTION 15

EIP COUNTER REPAIR AND RETURN FORM

TO FACILITATE REPAIRS, PLEASE ANSWER ALL QUESTIONS AND RETURN THIS FORM WITH COUNTER TO: EIP INCORPORATED, 3230 SCOTT BOULEVARD, SANTA CLARA, CA 95051.

MODEL NO. _____ SERIAL NO. _____

1. Briefly describe trouble symptoms: _____

   _____

2. Check frequency range in which trouble occured:
   Band I 20 Hz-135 MHz _____ Band I 10-300 MHz _____ Band II _____ Band III _____

3. Would the counter show the correct display in the TEST position? Yes ____ No _____.

4. What was the approximate ambient temperature? _____°F.

5. Did failure occur at turn on, or after some period of time? Turn on ____. After ____hours

6. At what frequency (ies) did counter fail to operate? _____.

7. What was the input power level at failure? _____ dBm (or mW).

8. Was the rear panel INT/EXT switch in the INT position? Yes _____ No _____.

9. What type of signal generator (or signal source) was being monitored by the counter at the time of failure? _____.

10. Please sketch (on the other side of this sheet), the test or operational set-up in use when the counter failed, and any additional comments regarding this instrument.

11. In the event counter repair cost is not covered under the EIP standard warranty, please complete the following:

    a. Maximum allowable charge without further customer approval: $ _____.

    b. P.O. No. _____ Date _____ Buyer _____.

    c. Billing address: _____

       _____.

12. Name of person making this report (PLEASE PRINT): _____.

    Your phone number: (Area Code: _____) _____ Ext: _____.

CUSTOMER INFORMATION	SHIPPING INFORMATION
OWNER _____	SHIP TO _____
ADDRESS _____	ADDRESS _____
CITY _____	CITY _____
STATE _____ ZIP _____	STATE _____ ZIP _____
COUNTRY _____	COUNTRY _____

EIP COUNTER REPAIR AND RETURN FORM

TO FACILITATE REPAIRS, PLEASE ANSWER ALL QUESTIONS AND RETURN THIS FORM WITH COUNTER TO: EIP INCORPORATED, 3230 SCOTT BOULEVARD, SANTA CLARA, CA 95051.

MODEL NO. _____ SERIAL NO. _____

1. Briefly describe trouble symptoms: _____

   _____

2. Check frequency range in which trouble occured:
   Band I 20 Hz-135 MHz _____ Band I 10-300 MHz _____ Band II _____ Band III _____

3. Would the counter show the correct display in the TEST position? Yes ____ No _____.

4. What was the approximate ambient temperature? _____ °F.

5. Did failure occur at turn on, or after some period of time? Turn on ____. After ____hours

6. At what frequency (ies) did counter fail to operate? _____.

7. What was the input power level at failure? _____ dBm (or mW).

8. Was the rear panel INT/EXT switch in the INT position? Yes _____ No _____.

9. What type of signal generator (or signal source) was being monitored by the counter at the time of failure? _____.

10. Please sketch (on the other side of this sheet), the test or operational set-up in use when the counter failed, and any additional comments regarding this instrument.

11. In the event counter repair cost is not covered under the EIP standard warranty, please complete the following:

    a. Maximum allowable charge without further customer approval: $ _____.

    b. P.O. No. _____ Date _____ Buyer _____.

    c. Billing address: _____

    _____.

12. Name of person making this report (PLEASE PRINT): _____.

    Your phone number: (Area Code: _____) _____ Ext: _____.

CUSTOMER INFORMATION	SHIPPING INFORMATION
OWNER _____	SHIP TO _____
ADDRESS _____	ADDRESS _____
CITY _____	CITY _____
STATE _____ ZIP _____	STATE _____ ZIP _____
COUNTRY _____	COUNTRY _____

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